SFAL

Semiconductor Fabless Accelerator Lab

Advanced Certification Program

SOC DESIGN AND IMPLEMENTATION

Duration: 6 Weeks Training

15 April 2024 – 4 June 2024

Additional 4 Weeks Specialized Program

Joint program by SFAL and VSD

6 Weeks Basic Training Program

Overview:

SFAL, in collaboration with VSD, is organizing a 10-weeks training program covering semiconductor design basics such as floorplanning, placement, CTS, routing, optimization, and verification. Students will learn everything from chip size estimation to signal integrity fixes. Following this, they will have the opportunity to choose a specialization topic, enabling targeted learning in a specific area of interest under expert guidance.

This blend of foundational learning, specialization, and practical application, guided by industry experts, prepares participants for successful careers in SoC design and implementation, balancing theoretical knowledge with hands-on experience.

WEEK 1

Floor planning

- Core and Die Size Determination – Understanding chip size estimation, aspect ratios, and setting margins.
- I/O Placement – Strategies for placing pads and I/O cells, package routing considerations.
- Power Planning – Designing a robust power distribution network, identifying power domains.
- Block Placement – Optimizing the placement of IP cores for performance and thermal management.

WEEK 2

Placement

- Initial Placement – Techniques for distributing cells across the chip.
- Optimization Cycles – Using iterative optimization to improve design metrics.
- Timing-Driven Placement – Adjusting cell positions based on timing analysis and constraints.

WEEK 3

Clock Tree Synthesis (CTS)

- Clock Tree Planning – Defining clock regions and skew minimization strategies.
- Clock Tree Implementation – Automated generation of clock tree, buffer, and inverter insertion.
- Skew and Jitter Optimization – Fine-tuning the clock tree for design targets.

WEEK 4

Routing

- Global Routing – Establishing routing guidelines and identifying congested areas.
- Detail Routing – Executing precise interconnect paths and resolving conflicts.
- Via Insertion – Optimizing via placements for performance and reliability.

WEEK 5

Post-Placement Optimization

- Buffer Insertion and Gate Sizing – Techniques for driving long wires and balancing drive strength.
- Logic Repositioning – Moving gates/cells to reduce critical path delays.

WEEK 6

Post-Route Optimization & Physical Verification

- Timing Closure Activities – Strategies for analyzing and fixing timing violations.
- Power Optimization – Techniques for reducing dynamic and static power consumption.
- Signal Integrity Fixes – Identifying and mitigating cross-talk and noise.
- Physical Verification – Performing DRC, LVS, and antenna checks.
- Extraction and Analysis – Parasitic extraction and post-layout simulation.

Advanced 4 Weeks Specialized Program

WEEK 7

Introduction to Chip Size Estimation

- Understand the fundamentals of chip size estimation, including the factors that influence size and the trade-offs involved.
- Analyze a given set of requirements for a hypothetical ASIC project and estimate the rough chip size based on technology node and basic functionality.

WEEK 8

Aspect Ratios and Layout Considerations

- Learn about aspect ratios, their impact on chip design, and how layout considerations affect aspect ratios.
- Given a set of functional blocks and their connections, propose an aspect ratio for a chip that optimizes for performance and cost, justifying your choices.

WEEK 9

Setting Margins and Design for Manufacturability

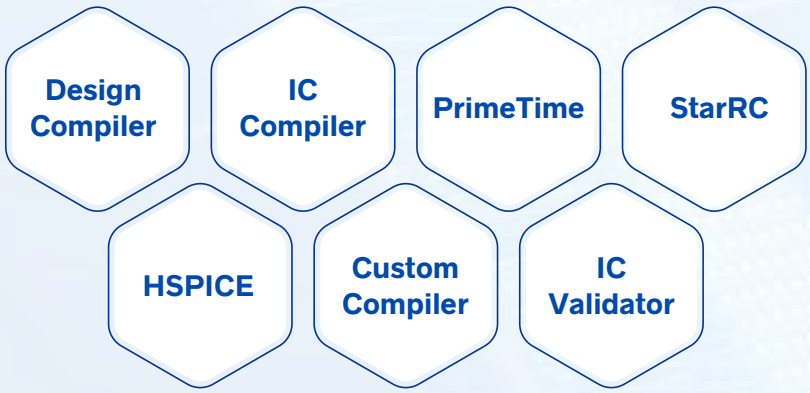
- Understand the fundamentals of chip size estimation, including the factors that influence size and the trade-offs involved.
- Create a margin plan for a provided chip design, detailing timing, power, and process margins. Include a rationale for each margin setting.

WEEK 10

Advanced Chip Size Optimization Techniques

- Delve into advanced techniques and tools used for chip size optimization and final determination.
- Using a case study of a chip with suboptimal size, propose optimization techniques to reduce the chip size while maintaining or improving its functionality.

Tools



EDA Partner

SYNOPSYS®

Why you should join this workshop

With SFAL, participants can advance their careers and transform their lives in impactful and real ways. Along with gaining a comprehensive understanding of SOC design and implementation, this 10-weeks program will also offer the following benefits to the students:

Collaborative Excellence

- Program execution by SFAL, VSD and Synopsys.
- Unique blend of academic and industry insights.

Customized Learning Journey

- Tailored topics for in-depth specialization.
- Direct mentorship from field experts.

Access to Industry Leaders

- Interactive sessions with seasoned professionals.
- Networking with industry pioneers.

Hands-On Project Experience

- Tackle real-world challenges through a design project.
- Build a comprehensive portfolio piece.

Gateway to Professional Growth

- Acquire skills in high demand across the semiconductor sector.
- Step into the professional world with potential internships.

Jointly Offered Program

- Collaboration between SFAL, VSD and Synopsys and supported by KDEM.
- Harnessing collective expertise and resources.

Career Opportunities

- Industry recognition for participants who have experience in chip tapeout.
- Understand how Time-to-market is crucial in this field.
- Opportunity to work directly on advanced analog, mixed-signal and RISC-V projects.

Cloud-Based Flexibility

- Self-paced learning.
- Simple login to week's lectures and labs.
- 24/7 Slack channel with over 150 teaching assistants.

Delivery Mode

- Easy-to-access labs, available through a virtual box image.
- Insightful Lectures on an Innovative LMS Platform.
- Round-the-Clock Q&A Support on Slack.
- Daily Check-in Calls for Direct Interaction.

Eligibility

- 3rd Year / Final Year Students, Recently Graduated / Freshers or Experienced Professionals interested in core specialization.
- Atleast BE/BTech/ME/MTech or equivalent.

Instructor Profile

KUNAL GHOSH

Co-founder, VLSI System Design (VSD)

The co-founder of VLSI System Design (VSD) Corp. Pvt. Ltd., stands at the forefront of online open-source EDA and hardware design education, particularly in the realm of RISC-V.

With a portfolio of 50 top-tier VLSI online courses, Kunal has enriched the learning journey of over 90,000 students across 153 countries. His expertise extends beyond training and is actively involved in pioneering open-source projects and design collaborations with many institutions. He holds a master's degree from IIT Bombay, where he specialized in VLSI & Nano-electronics, with a focus on sub-100nm Electron Beam Lithography Optimization techniques.

About Us

Semiconductor Fabless Accelerator Lab (SFAL), is a K-Tech CoE for the Fabless community. An initiative funded by the Department of Electronics, IT, Bt, and S&T of Government of Karnataka through its Karnataka Innovation Technology Society (KITS), in collaboration with India Electronics and Semiconductor Association (IESA) towards developing and enhancing the fabless ecosystem in India. The focus of SFAL is around enabling fabless startups, across India and encouraging the creation and development of Products/IPs from India.

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SFAL Semiconductor Fabless Accelerator Lab

For more details visit

https://www.vlsisystemdesign.com/sfal/