TCL Programming Project using openMSP430 - a synthesizable 16bit micro-controller core

TCL scripting project is an unique application to feed the design details (like constraints, libraries, netlist) in an Excel sheet format and generate pre-layout timing results. This is a general practice followed in VLSI industries. The UI ‘vsdsynth’ can be downloaded from below link, and view the README file to run ‘vsdsynth’. Currently, 'vsdsynth’ is tested using openMSP430.

Further versions of this UI are still under developing that can be applied on any design. This project is to learn TCL programming from scratch and to create EDA commands like read_sdc, read_lib, and many more. User can be re-coded this UI for University VLSI projects or applications.

'vsdflow' is also the best utility ever written for learning EDA based TCL scripting.

VSDFLOW is an automated solution to programmers, hobbyists and small scale semiconductor technology entrepreneurs who can craft their ideas in RTL language, and convert the design to hardware using VSD (RTL-to-GDS) FLOW. VSDFLOW is completely build using OPHW tools, where the user gives input RTL in verilog. From here on the VSDFLOW takes control, RTL is synthesized (using Yosys).

The synthesized netlist is given to PNR tool (Qflow) and finally Sign-off is done with STA tool (using Opentimer). The output of the flow is GDSII layout and performance & area metrics of your design. VSDFLOW also provide hooks at all stages for users working at different levels of design flow. It is tested for 30k instance count design like ARM Cortex-M0, RISC-V picorv32, and can be further tested for multi-million instance count using hierarchical or glue logic.
Its updated and now available for download for FREE...Here's the link:
https://github.com/kunalg123/vsdflow