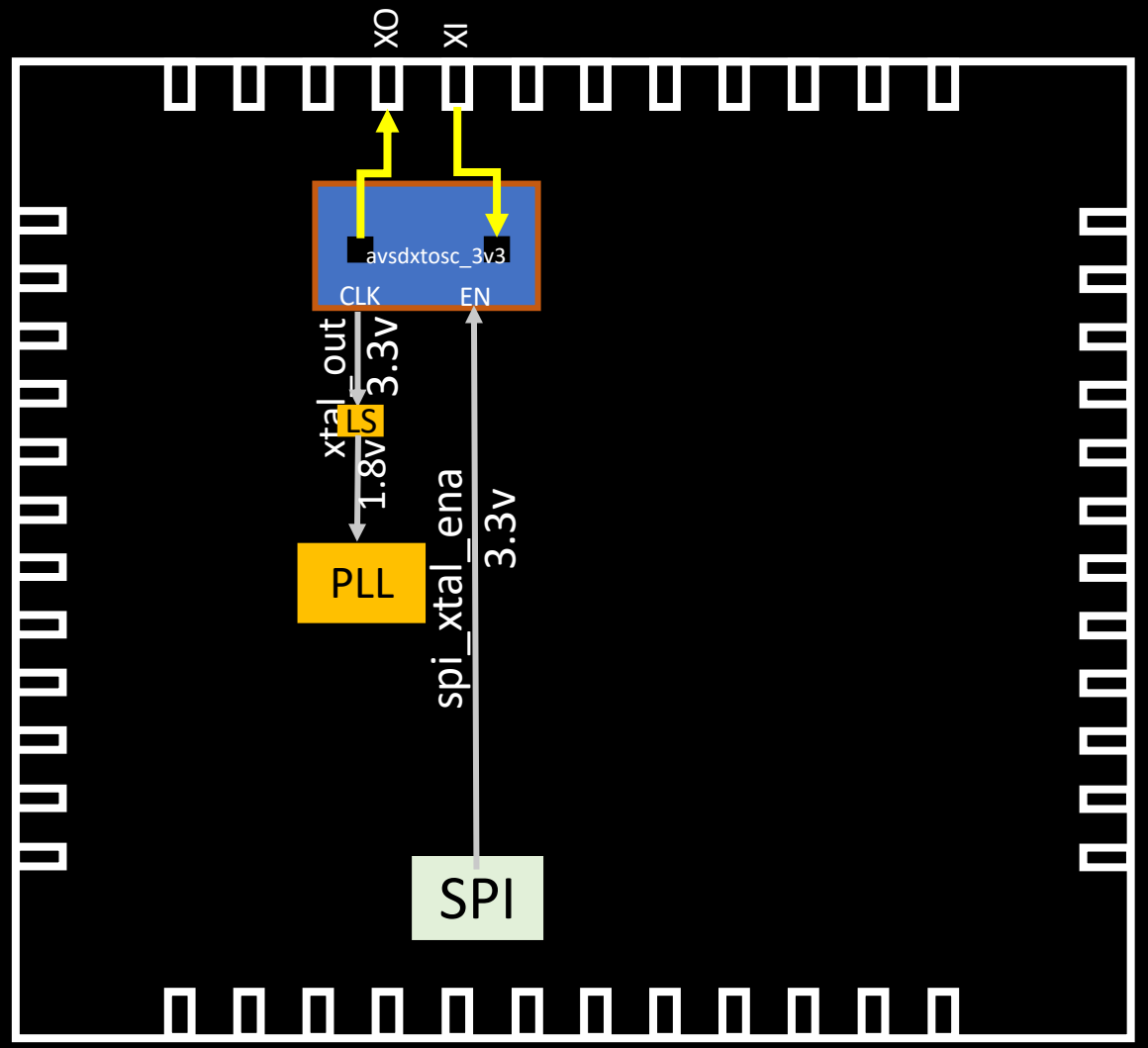
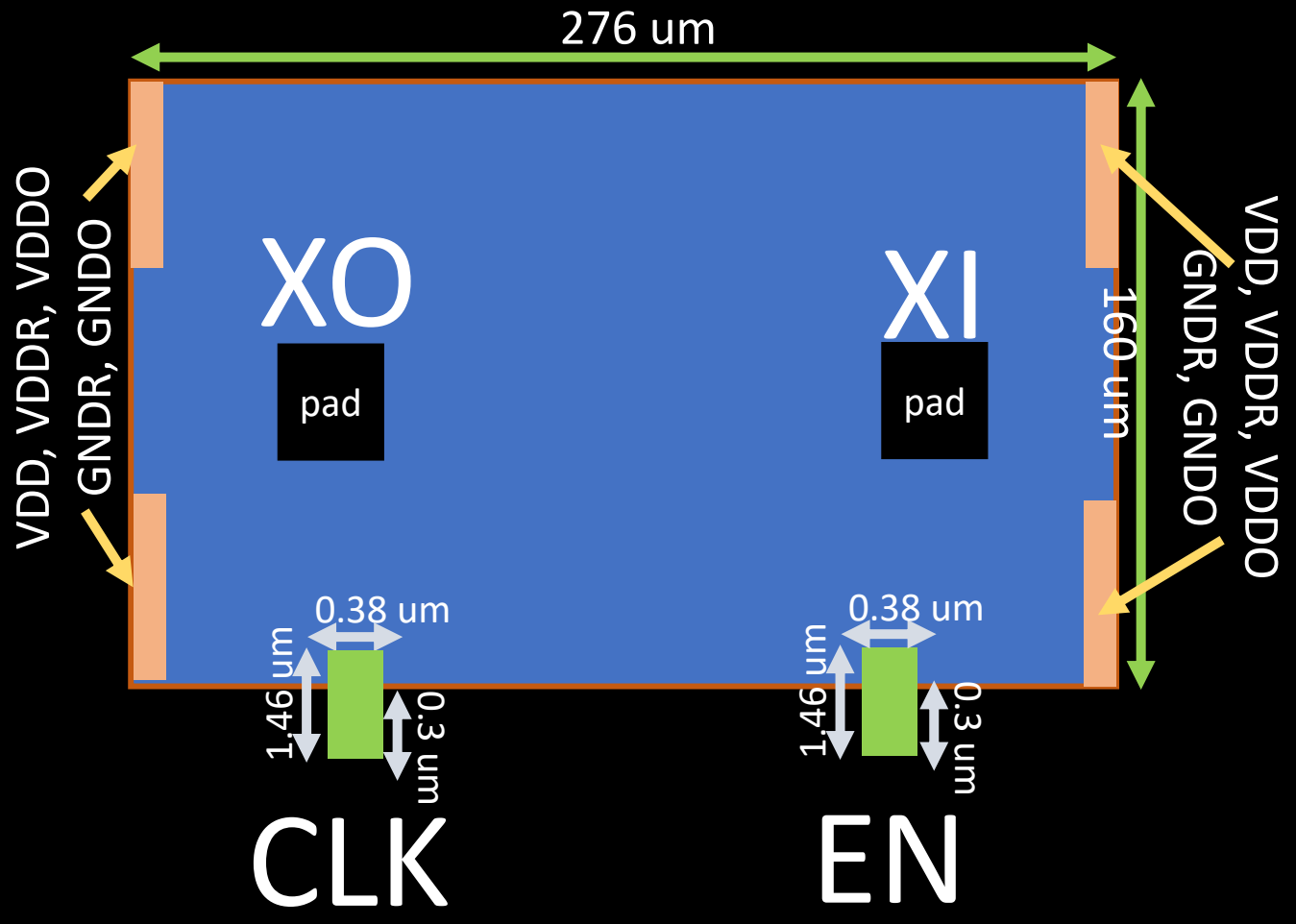
Crystal oscillator analog pad (avsdxtosc_3v3) spec sheet for 180nm tech node

- Specs released under APACHE LICENSE 2.0
- Please contact Kunal at kunalpghosh@gmail.com in case of any doubts

Application Note for crystal oscillator analog pad (avsdxtosc_3v3)

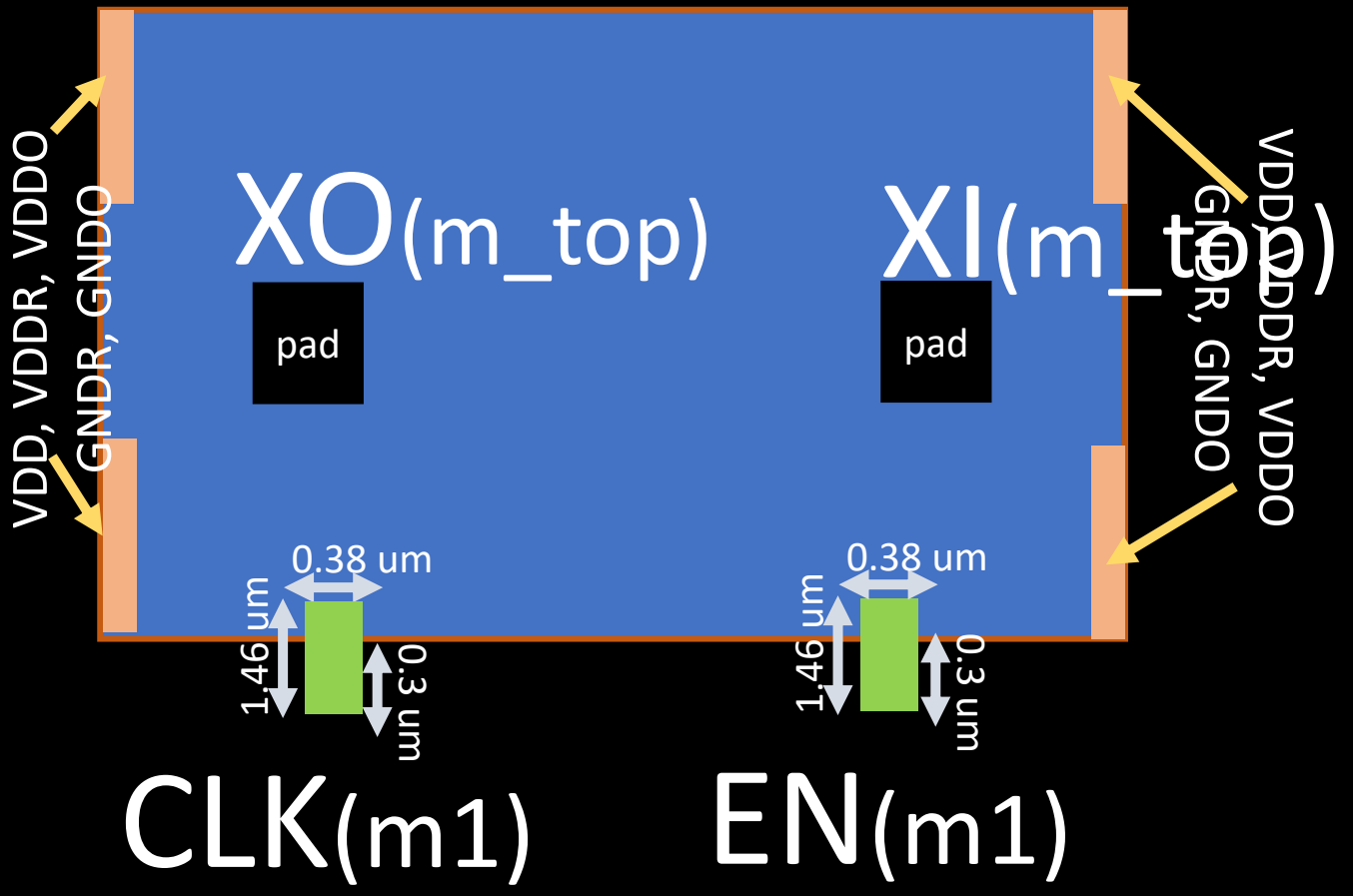


avsdxtosc_3v3
preferred dimensions and pin locations



avsdxtosc_3v3
preferred metal layers

VDD – m_top
VDDR – m2 and m_top
VDDO – m2 and m_top
GNDR – m_top
GNDO – m2 and m_top



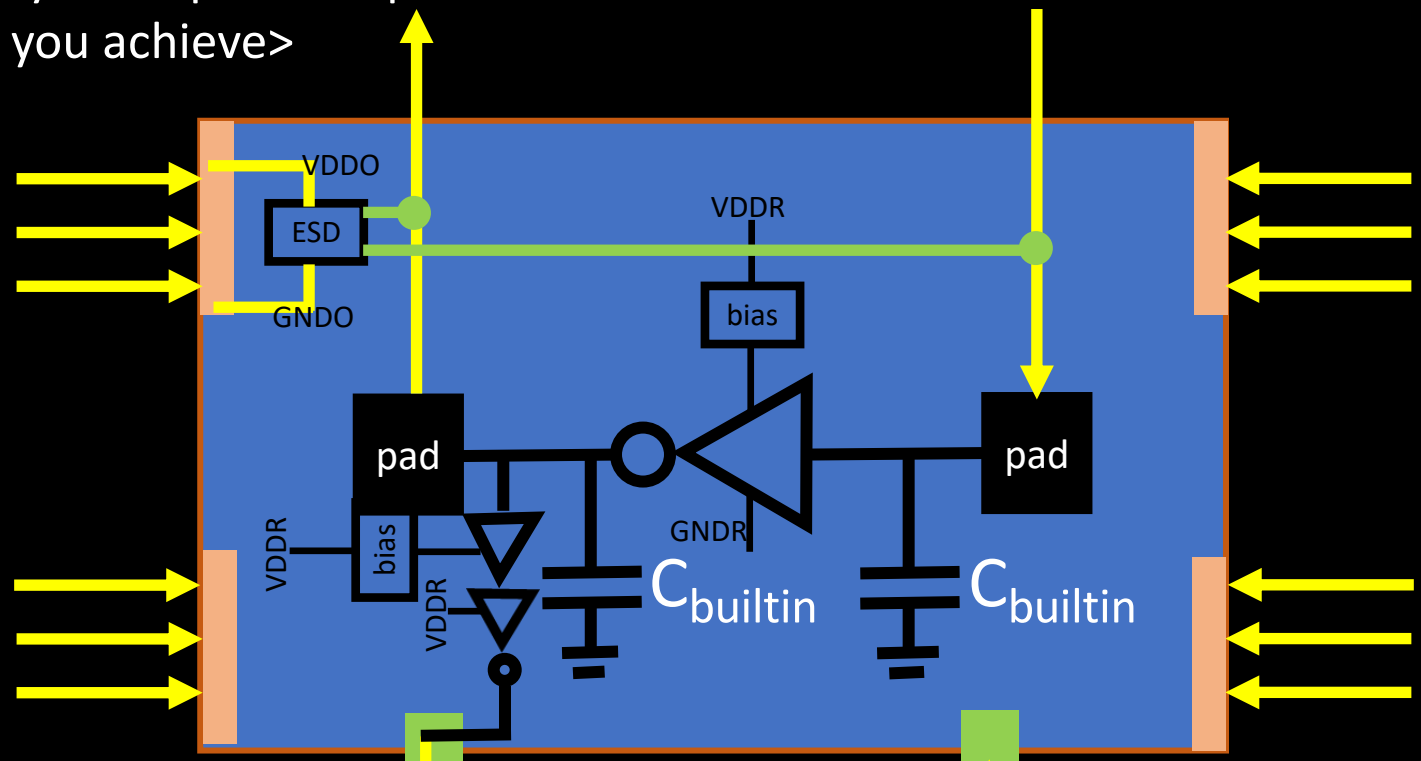
avsdxtosc_3v3 Timing specs

F_{min} = (inv) of 1MHz
F_{max} = (inv) of 8MHz
Duty cycle = <please report what you achieve>

XO

XI

F_{min} = 1MHz
F_{max} = 8MHz
Duty cycle = 50%



VDD – 1.8v
VDDR – 3.3v
VDDO – 3.3v
GNDR – 0v
GNDO – 0v

VDD – 1.8v
VDDR – 3.3v
VDDO – 3.3v
GNDR – 0v
GNDO – 0v

$C_{builtin}$ ~ 12pF

Logic '1'

Logic '0'

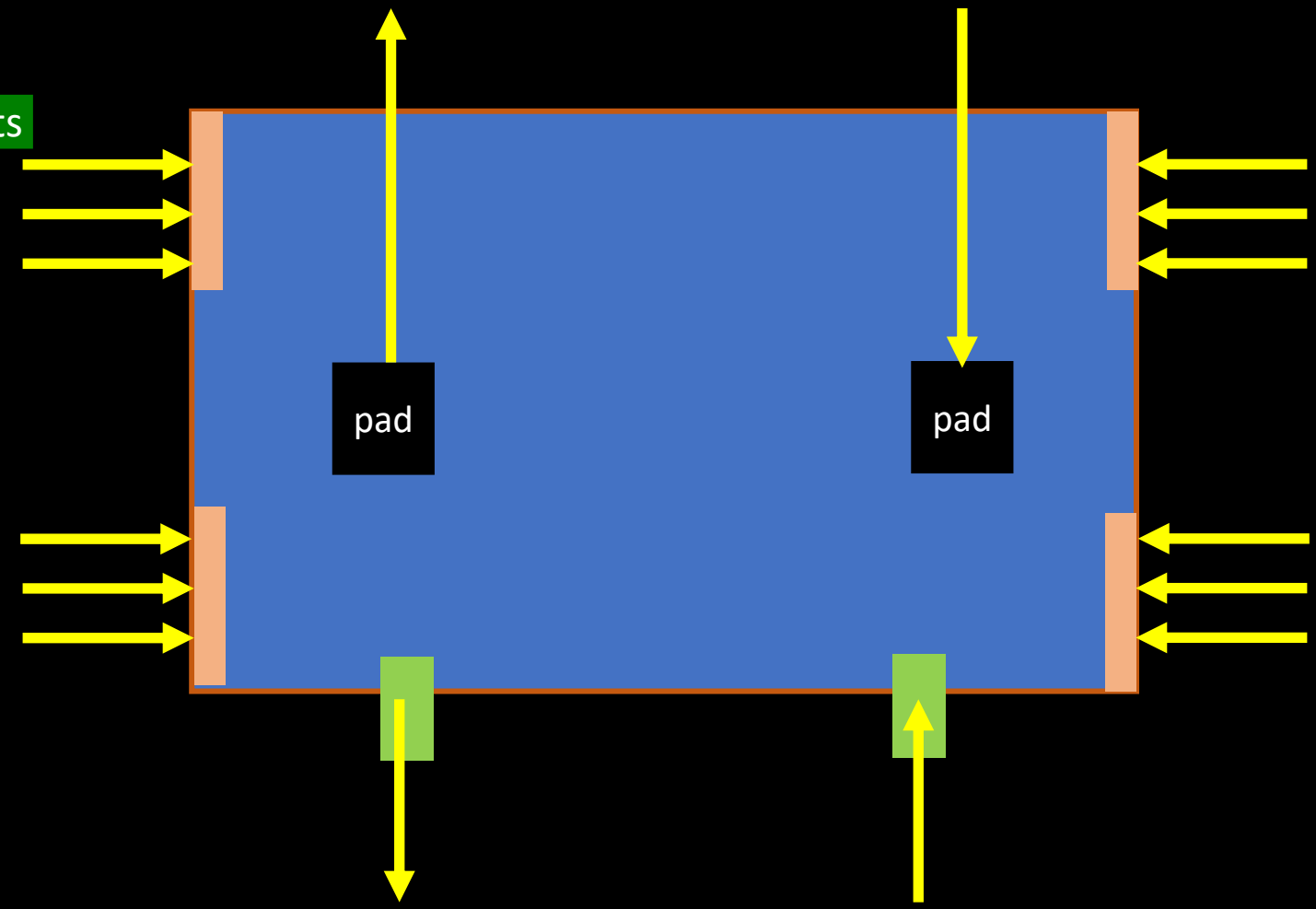
F_{clkmin} = 1MHz, when EN=1
F_{clkmax} = 4MHz, when EN=1
Duty cycle = <please report what you achieve>

CLK

EN

avsdxtosc_3v3 imp notes

VDD is present in layout to connect to overall IO ring of chip. They are NOT connected to circuit and don't influence its operation



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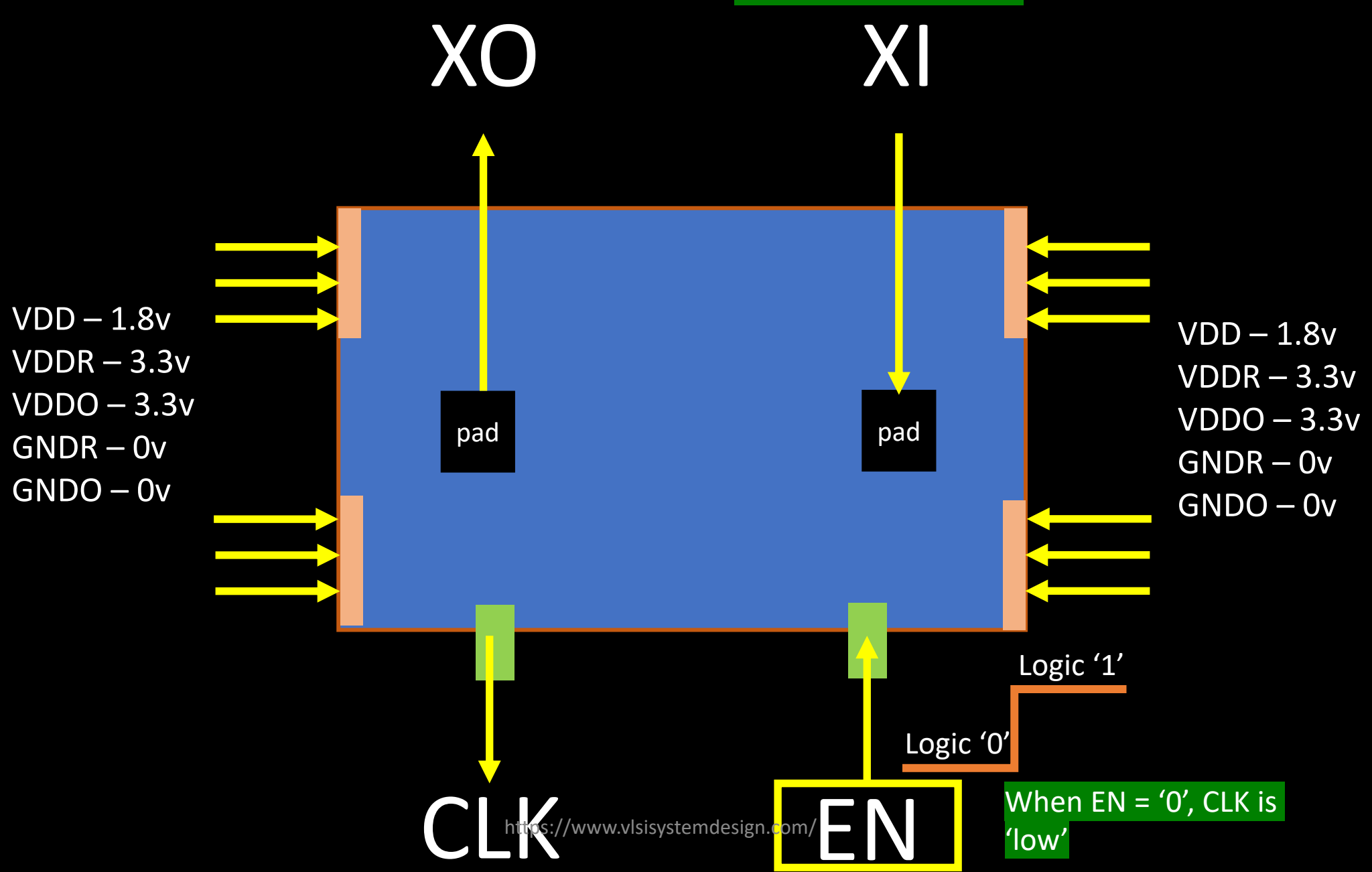
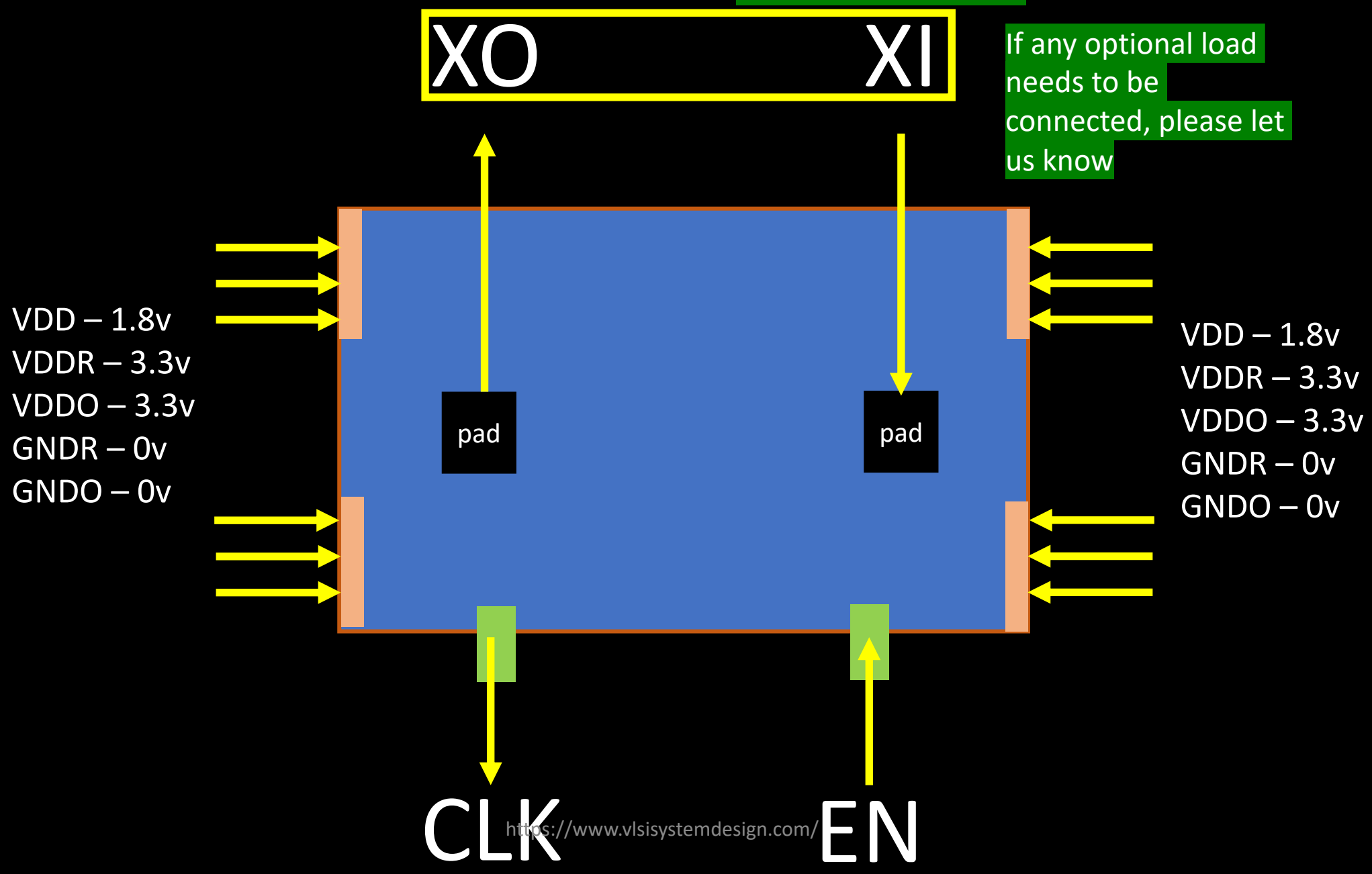
avsdxtosc_3v3 imp notes



avsdxtosc_3v3 imp notes



avsdxtosc_3v3 plots needed

1) IDD vs [F_{clkmin} to F_{clkmax}] at VDDR = 3.3v
2) Duty cycle vs [F_{clkmin} to F_{clkmax}] at VDDR = 3.3v
3) IDD vs VDDR[2V to 4V] at F_{clk}=2MHz, F_{clk}=4MHz, F_{clk}=6MHz and F_{clk}=8MHz
4) Duty cycle vs VDDR[2V to 4V] at F_{clk}=2MHz, F_{clk}=4MHz, F_{clk}=6MHz and F_{clk}=8MHz