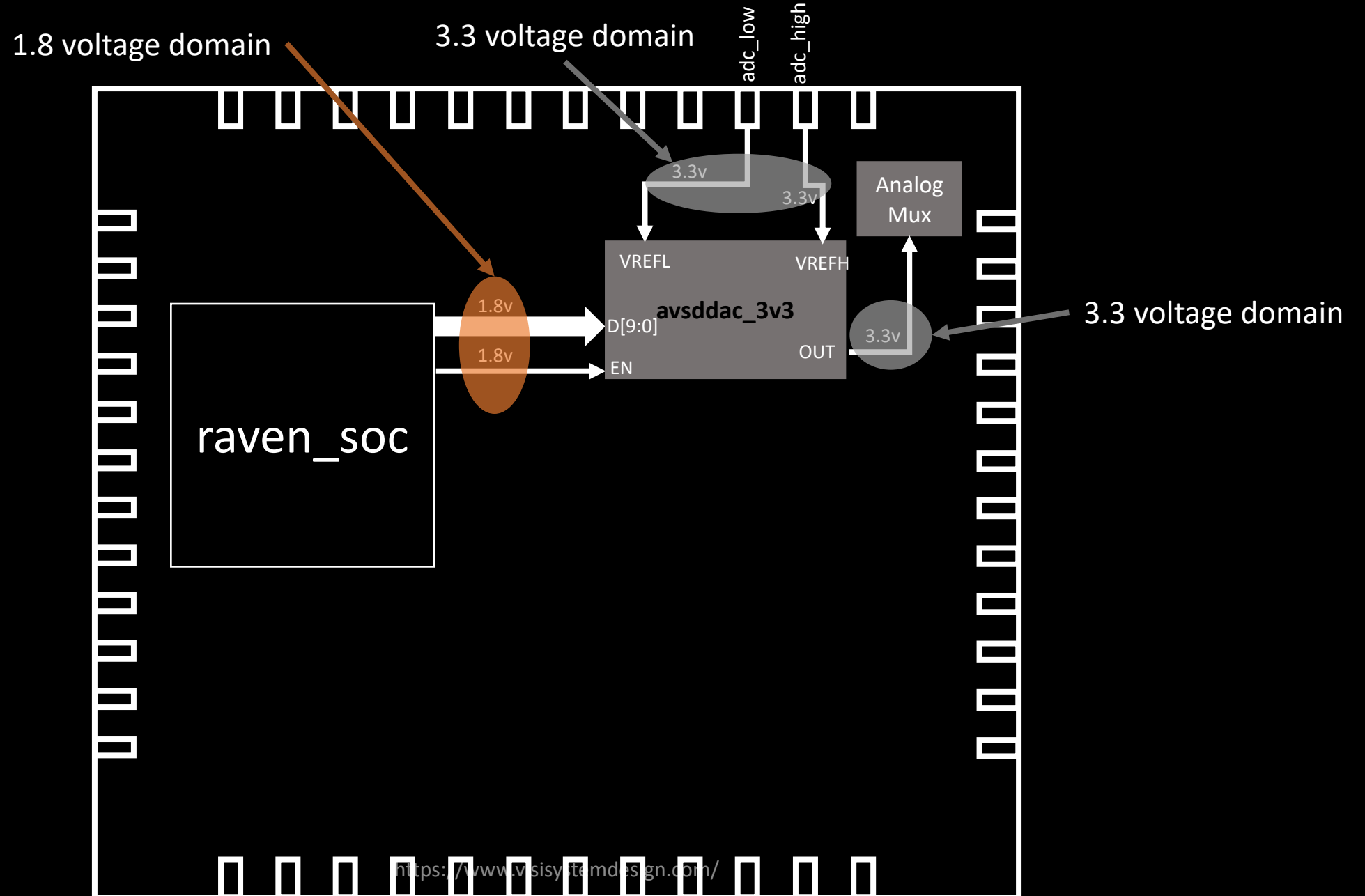


# DAC (avsddac\_3v3) spec sheet for 180nm tech node

- Specs released under **APACHE LICENSE 2.0**
- Please contact Kunal at [kunalpghosh@gmail.com](mailto:kunalpghosh@gmail.com) in case of any doubts

# Application Note for dac (avsddac\_3v3)



# avsdac\_3v3 preferred dimensions, pin locations and metal layers



 VDD, VSS pins (metal2) – 1.5 $\mu\text{m}$  x 0.8 $\mu\text{m}$

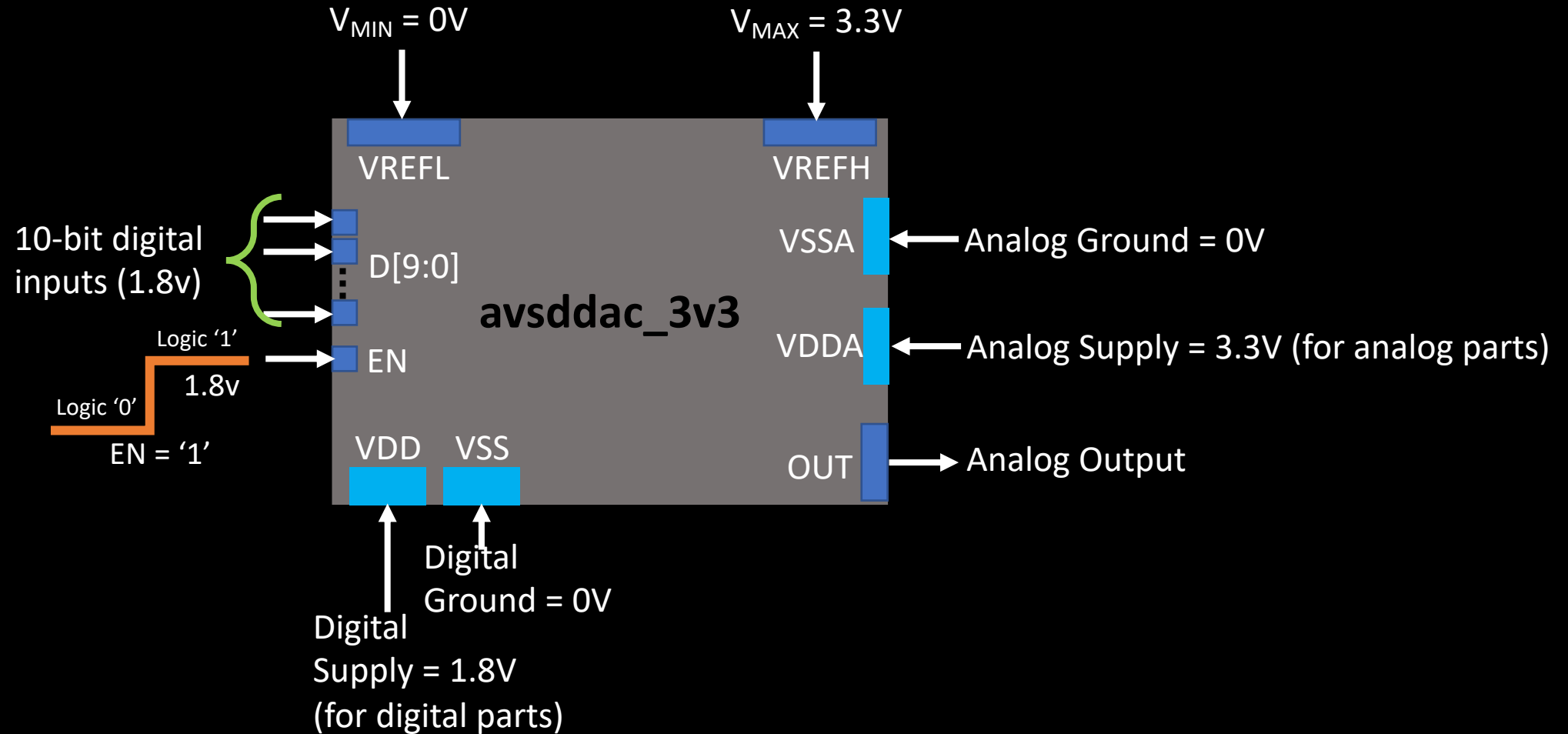
 VREFL, VREFH pins (metal2) – 9.48 $\mu\text{m}$  x 0.8 $\mu\text{m}$

 D[9-0], EN pins (metal3) – 0.28 $\mu\text{m}$  x 0.28 $\mu\text{m}$

 OUT pin (metal3) – 0.8 $\mu\text{m}$  x 1.6 $\mu\text{m}$

 VDDA, VSSA pins (metal3) – 0.8 $\mu\text{m}$  x 3 $\mu\text{m}$

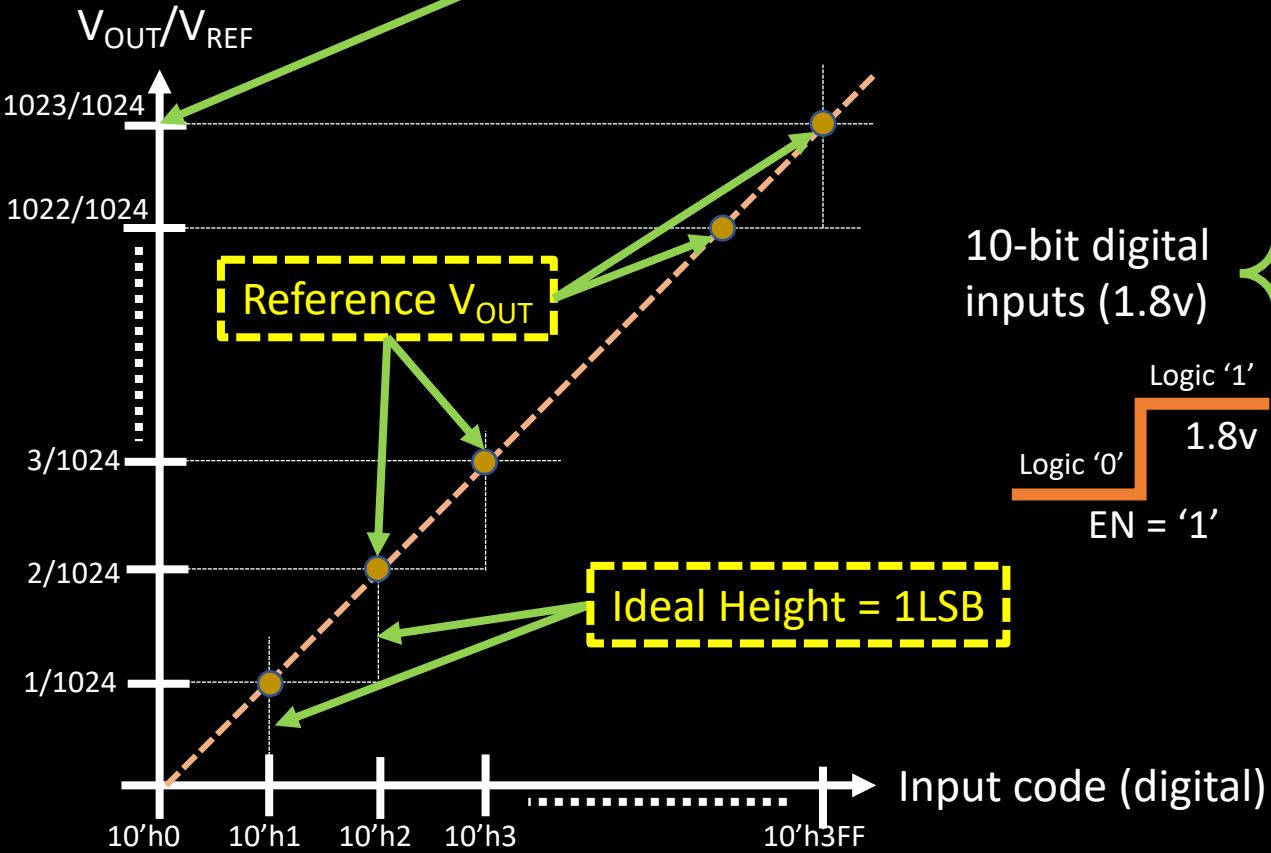
# avsdac\_3v3 operating modes



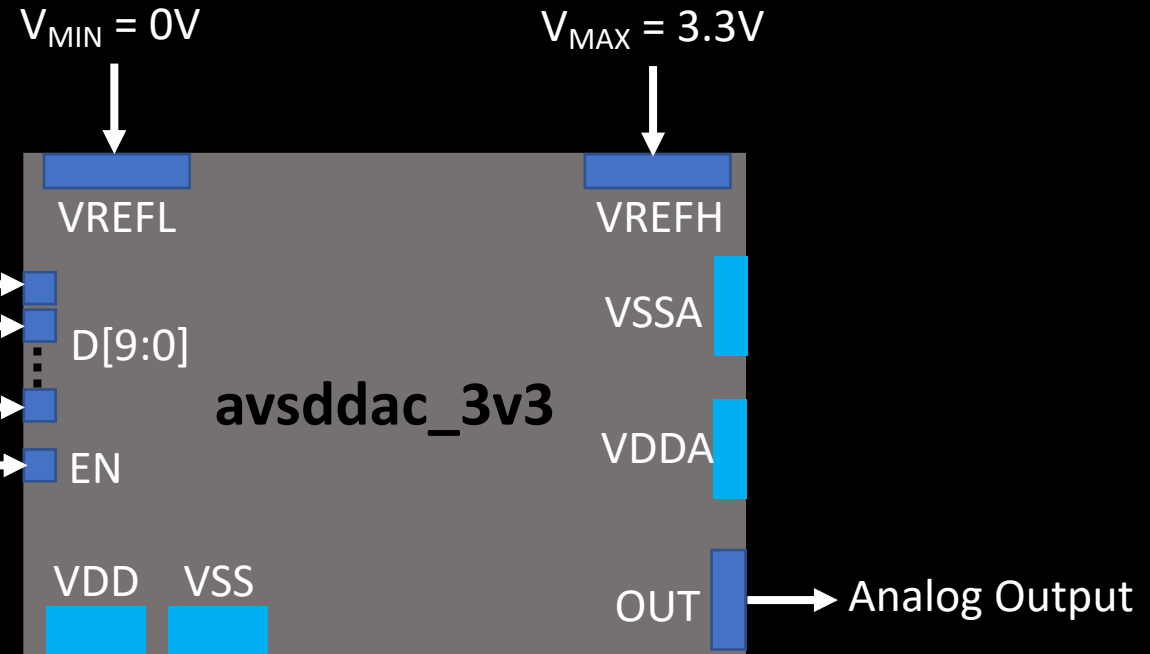
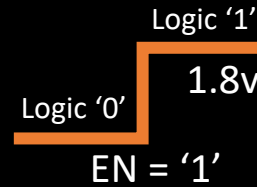
# avsdac\_3v3 operating modes

Full scale voltage  
 $V_{FS} = 0V \text{ to } 3.297V$

Accuracy = 0.09%



10-bit digital inputs (1.8v)



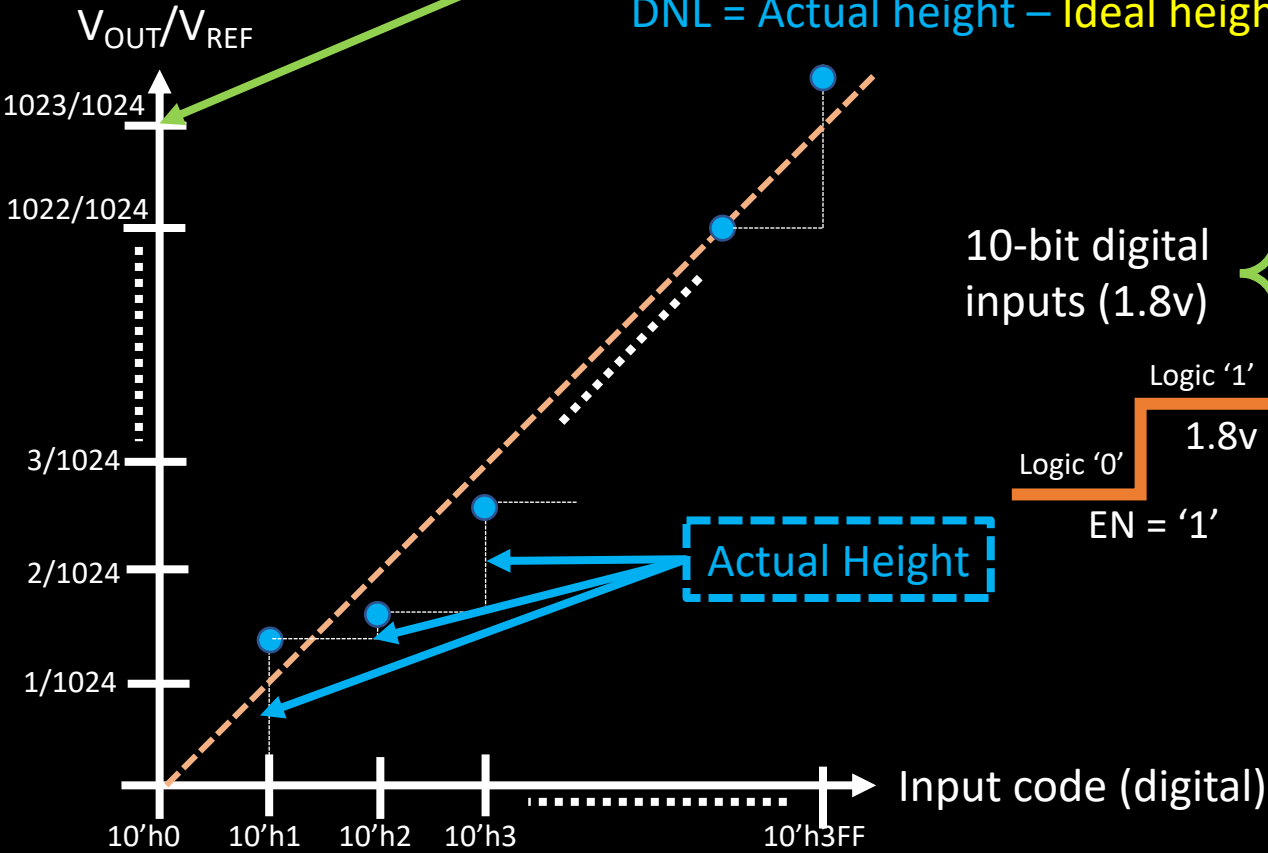
1LSB = 0.00322V or 3.2mV ( $1LSB = V_{REF}/2^N$ )  
Resolution = 10bits (For  $V_{REF}=3.3V$ )

# avsdac\_3v3 operating modes

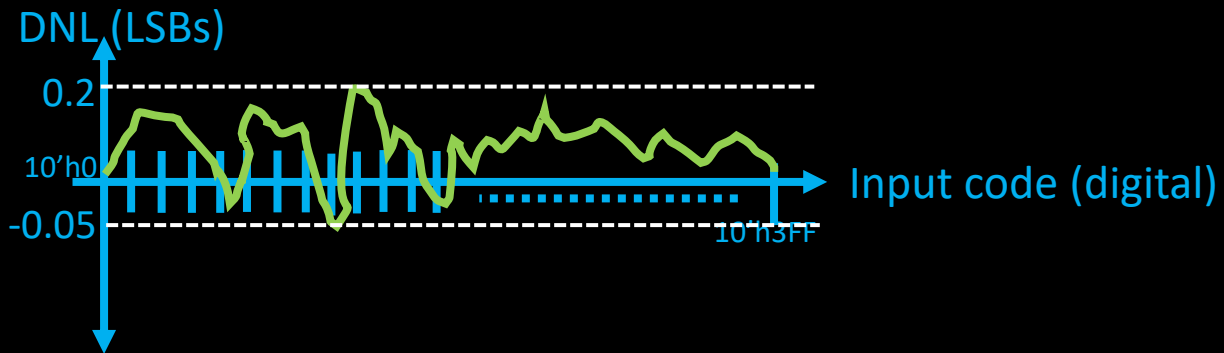
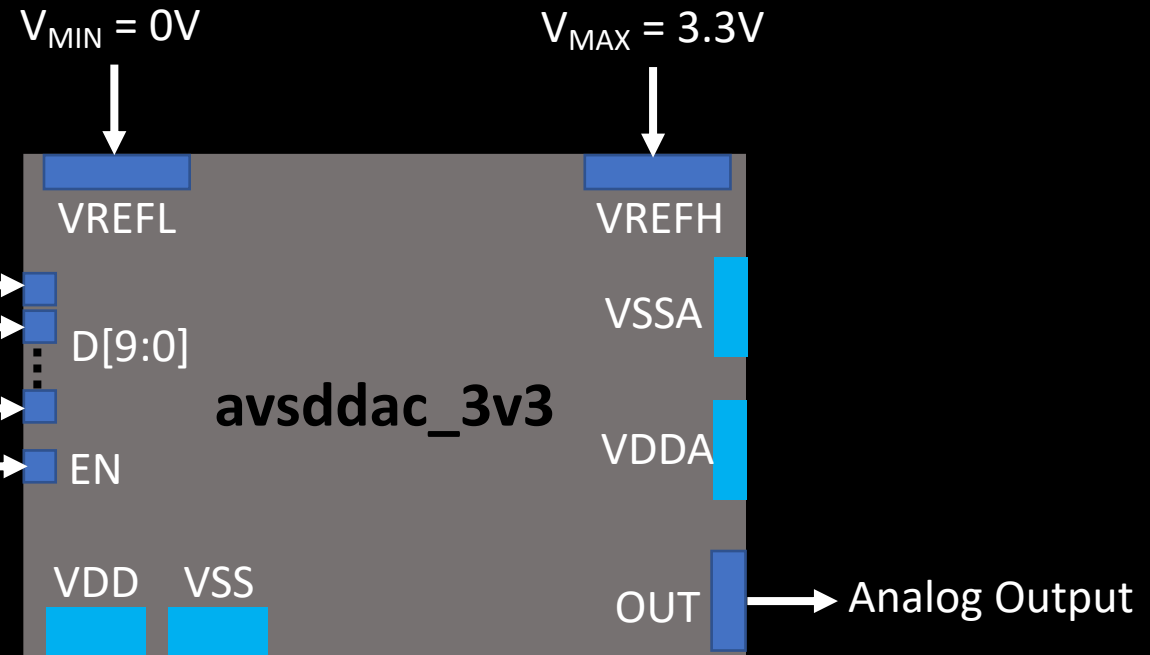
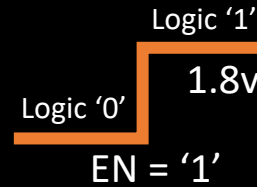
Full scale voltage  
 $V_{FS} = 0V \text{ to } 3.297V$

Differential nonlinearity  
(DNL) = 0.2LSB

DNL = Actual height - Ideal height



10-bit digital  
inputs (1.8v)

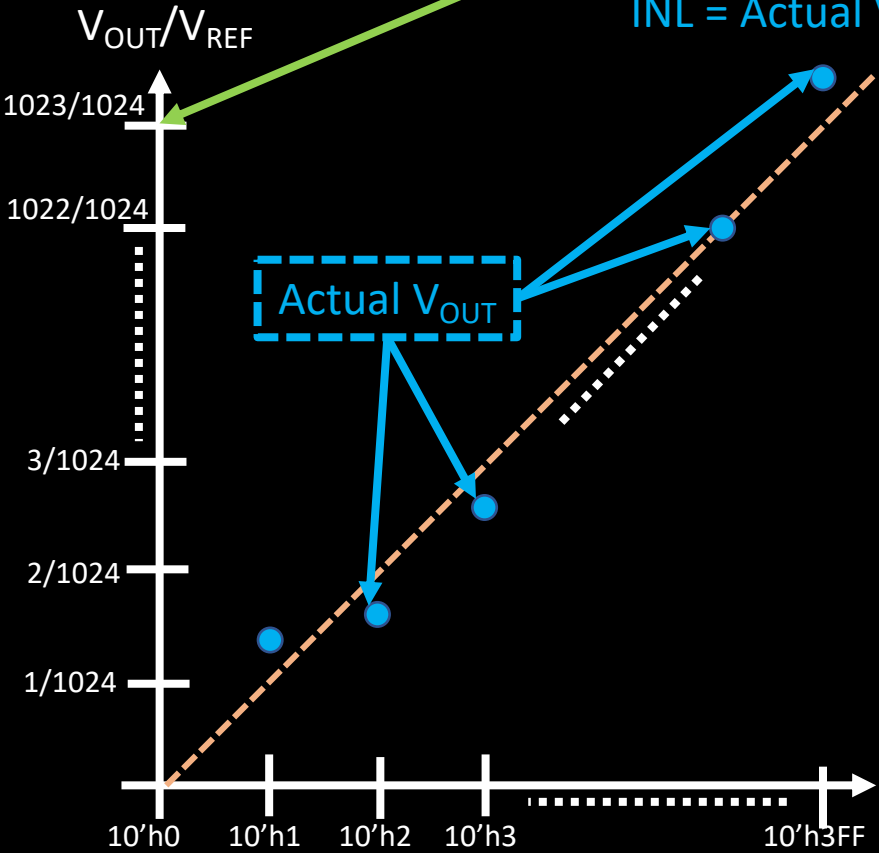


# avsdac\_3v3 operating modes

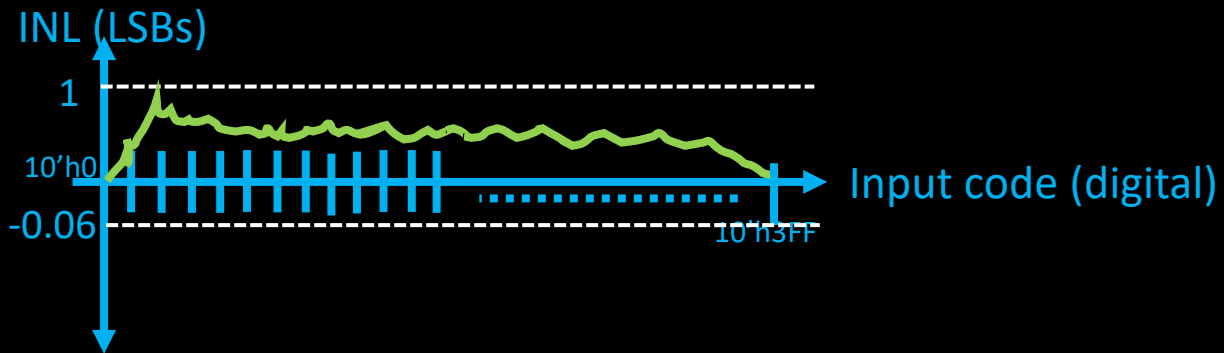
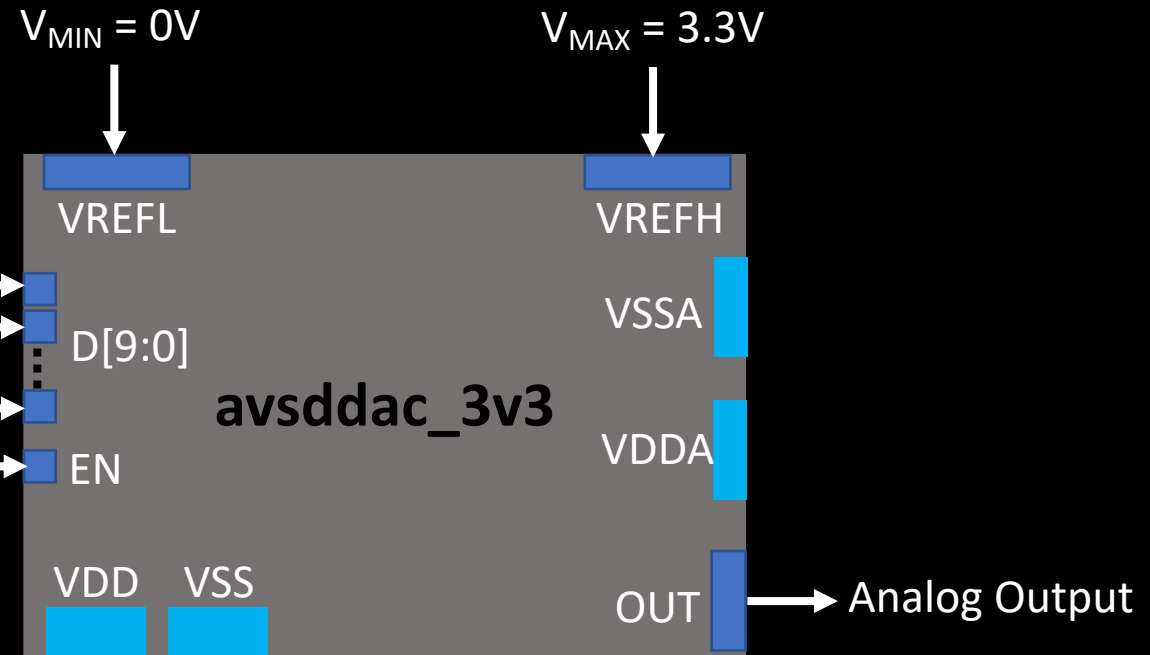
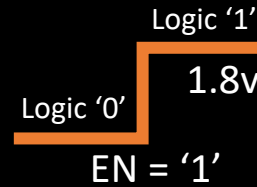
Full scale voltage  
 $V_{FS} = 0V \text{ to } 3.297V$

Integral nonlinearity  
(INL) = 1LSB

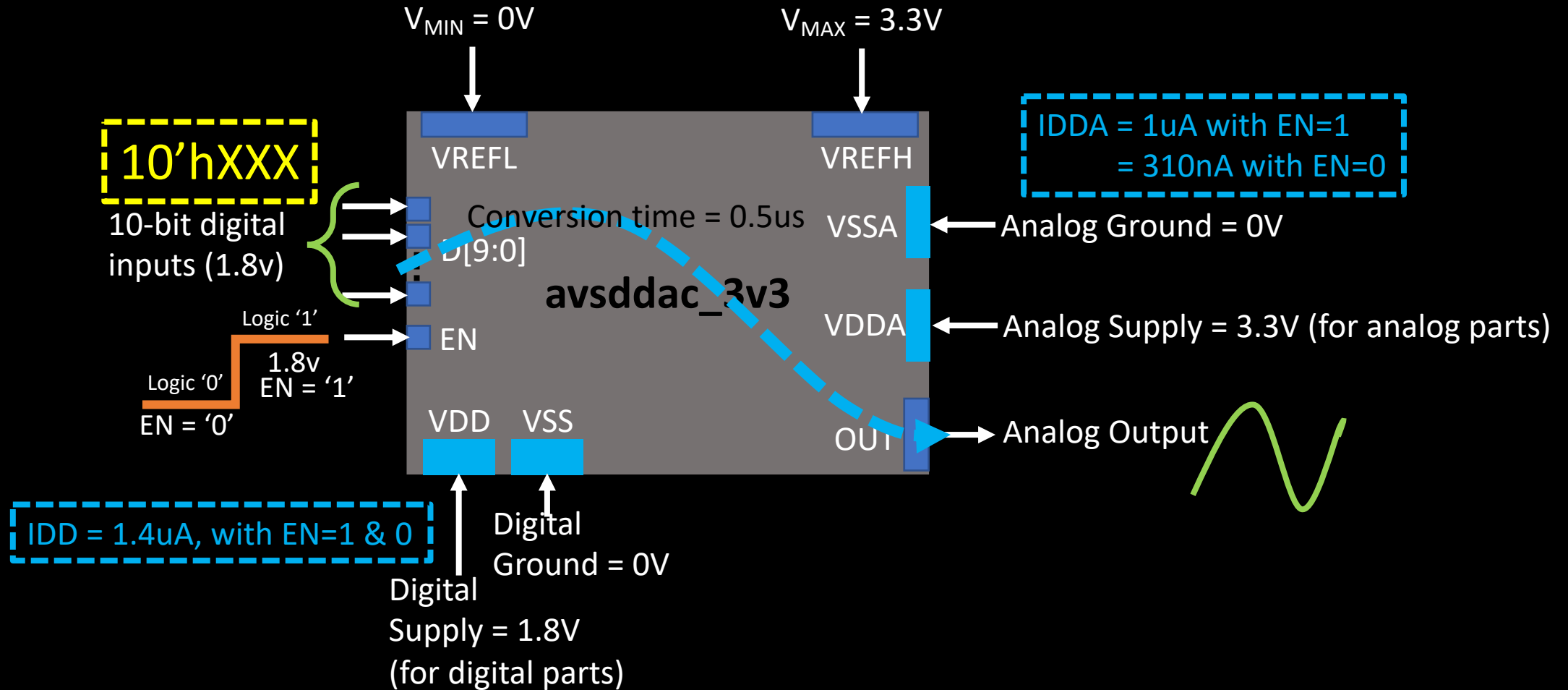
$$INL = \text{Actual } V_{OUT} - \text{Reference } V_{OUT}$$



10-bit digital  
inputs (1.8v)



# avsdac\_3v3 operating modes





## avsdac\_3v3 plots and values needed

- 1) DNL vs Digital code at  $V_{REF}=V_{DD}=3.3V$  and  $T=20C$  &  $85C$
- 2) INL vs Digital code at  $V_{REF}=V_{DD}=3.3V$  and  $T=20C$  &  $85C$
- 3) DNL vs Digital code at  $V_{REF}=1.25V$ ,  $V_{DD}=3.3V$  and  $T=20C$  &  $85C$
- 4) INL vs Digital code at  $V_{REF}=1.25V$ ,  $V_{DD}=3.3V$  and  $T=20C$  &  $85C$