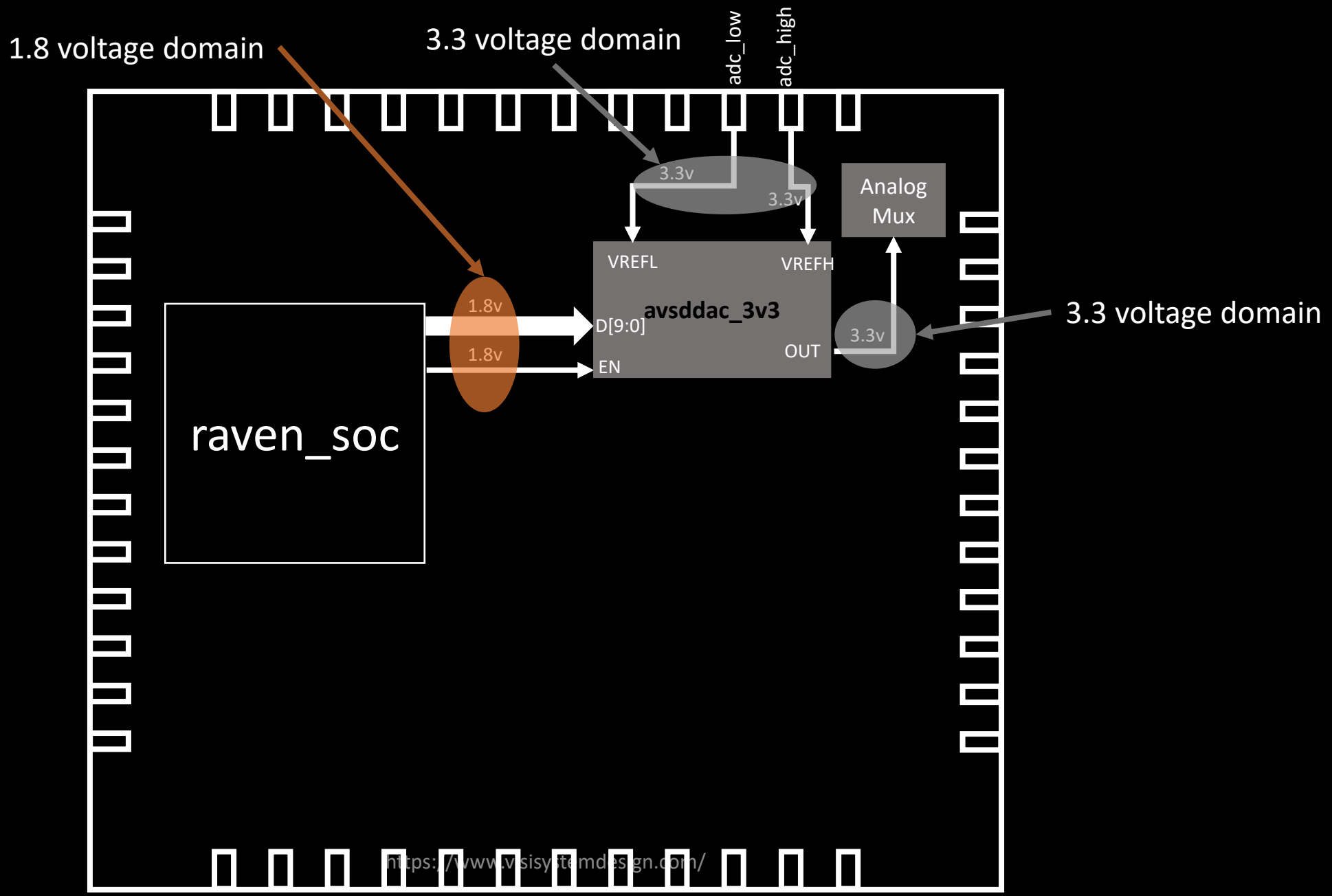
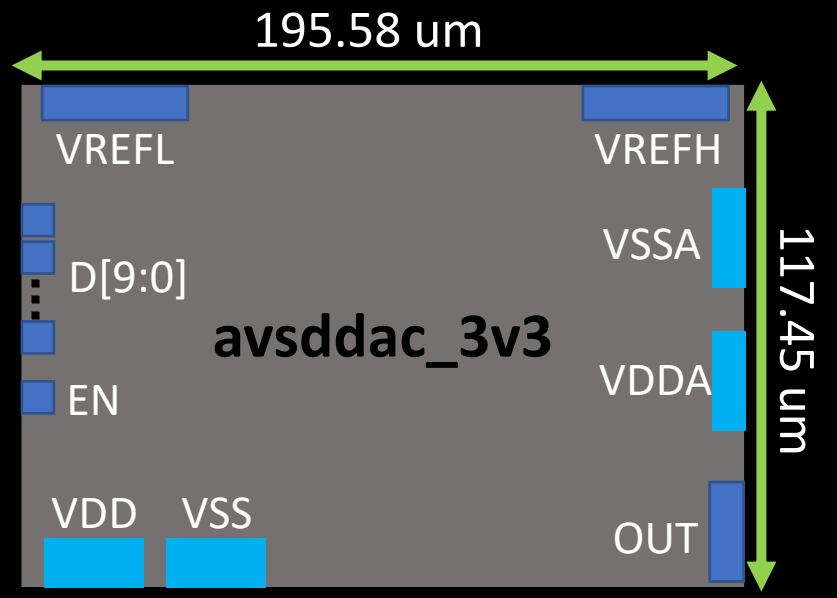
DAC (avsddac_3v3) spec sheet for 180nm tech node

- Specs released under APACHE LICENSE 2.0
- Please contact Kunal at kunalpghosh@gmail.com in case of any doubts

Application Note for dac (avsddac_3v3)



avsddac_3v3 preferred dimensions, pin locations and metal layers



VDD, VSS pins (metal2) – 1.5um x 0.8um

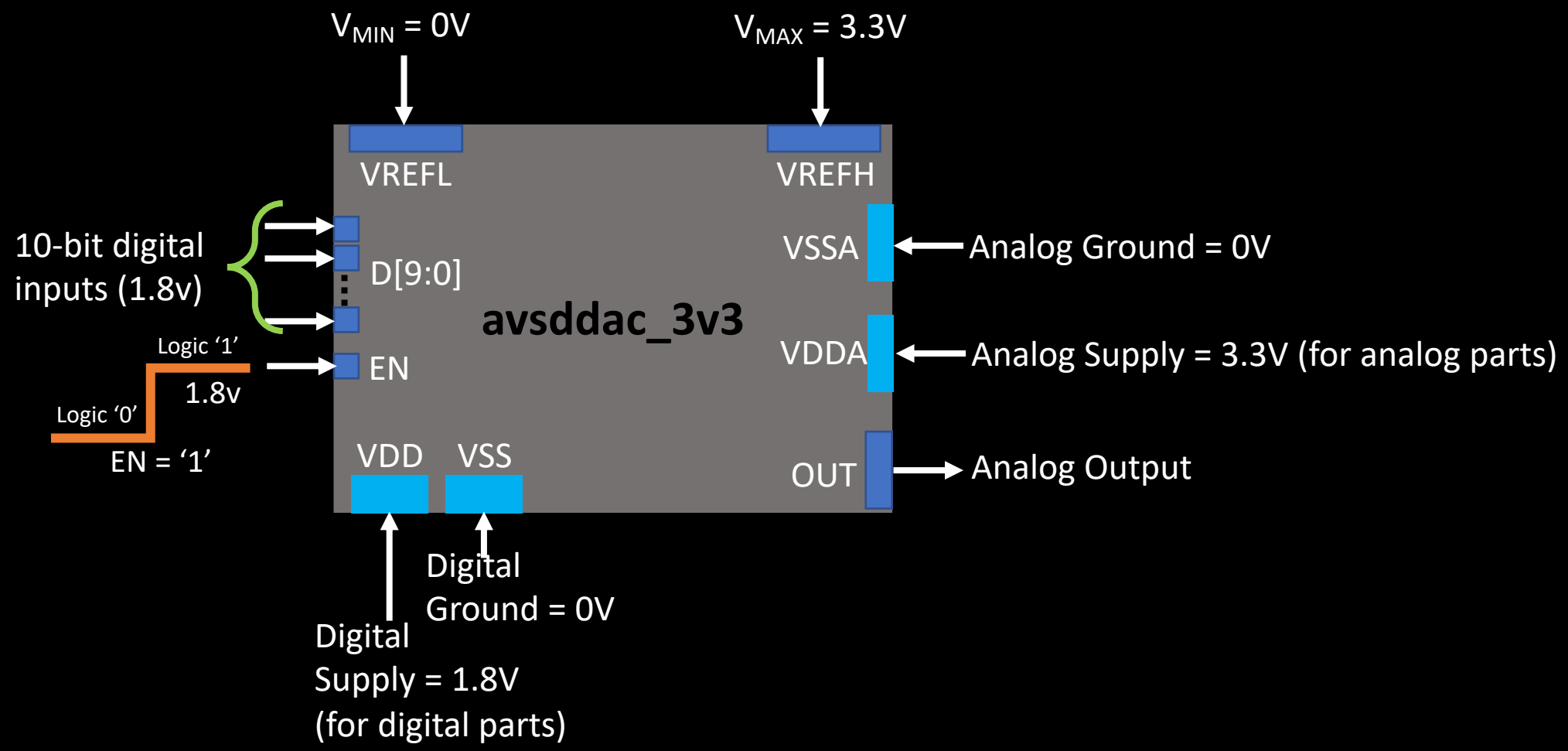
D[9-0], EN pins (metal3) – 0.28um x 0.28um

VREFL, VREFH pins (metal2) – 9.48um x 0.8um

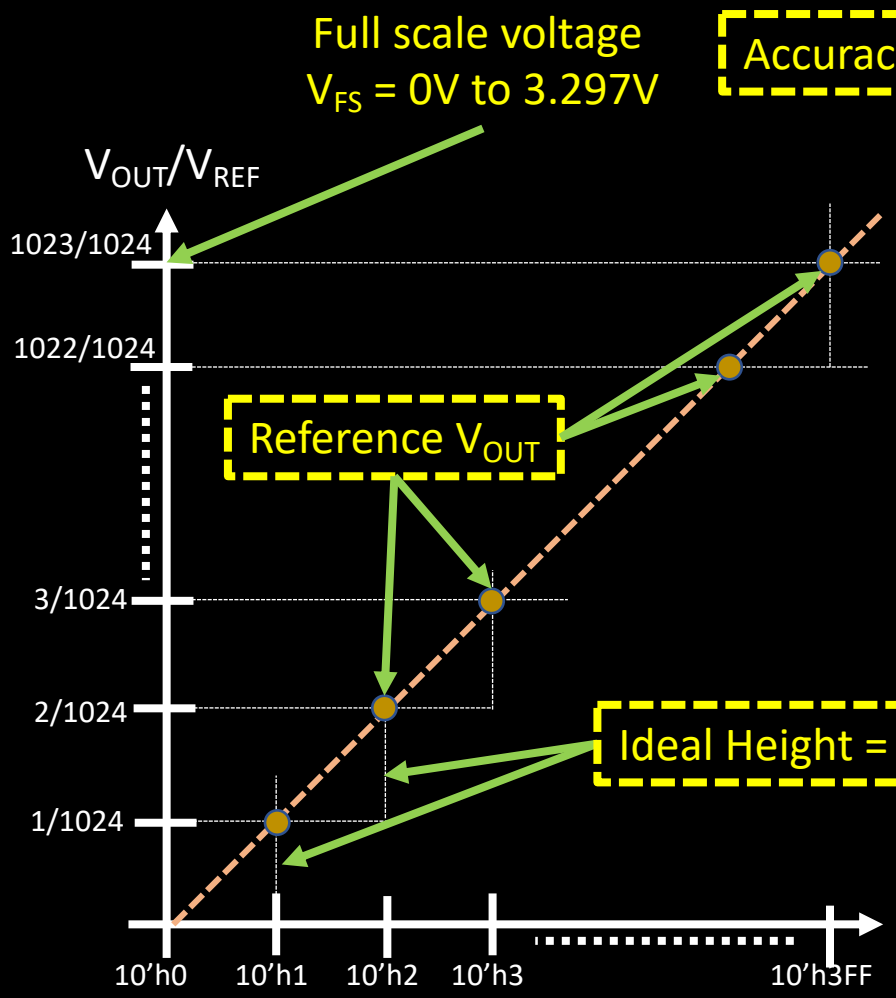
OUT pin (metal3) – 0.8um x 1.6um

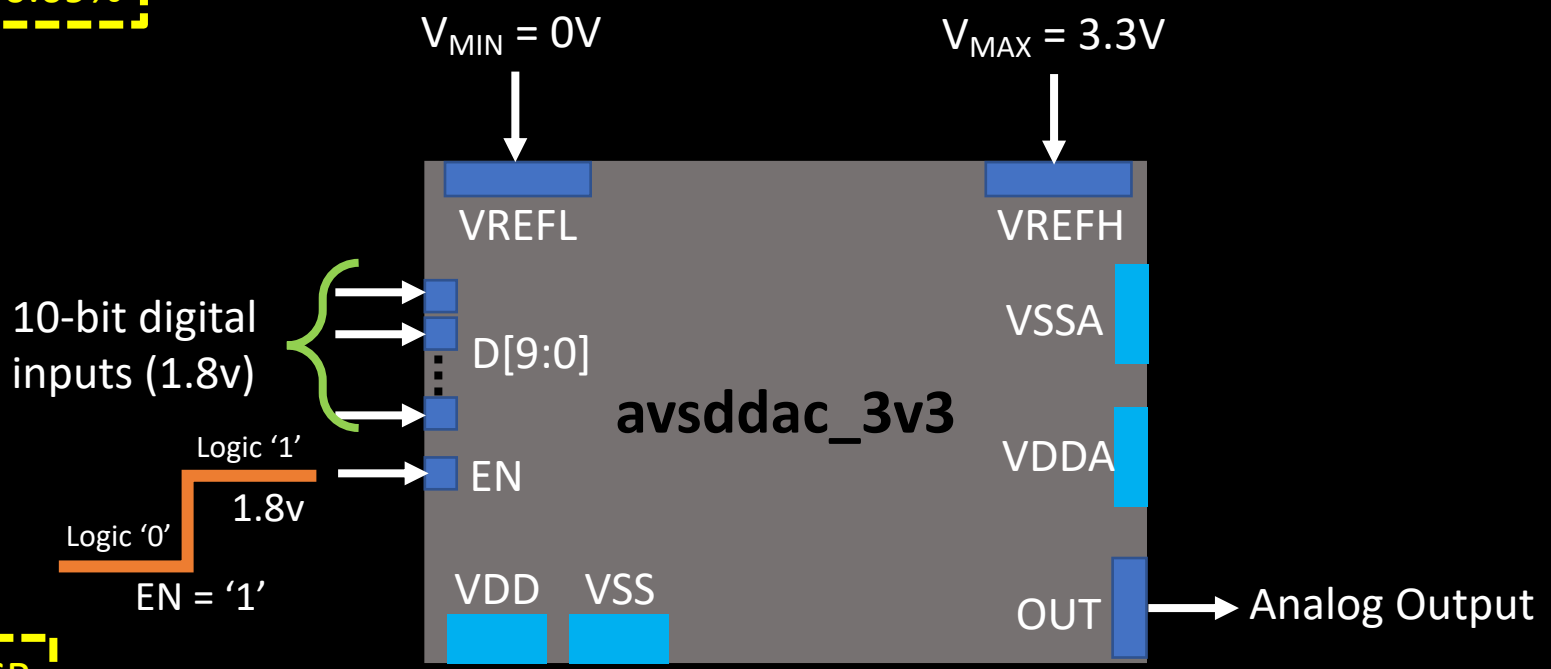
VDDA, VSSA pins (metal3) – 0.8um x 3um

avsddac_3v3 operating modes



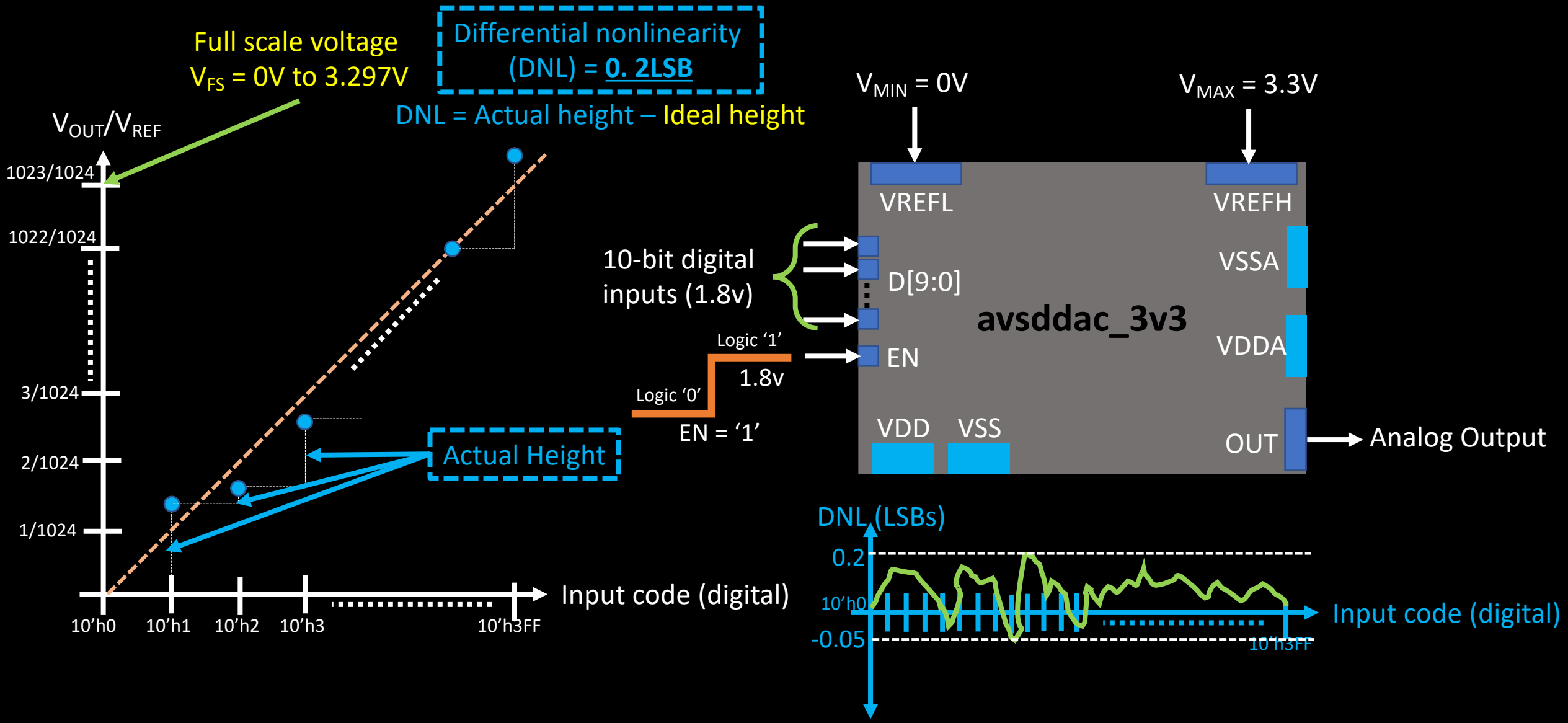
avsddac_3v3 operating modes



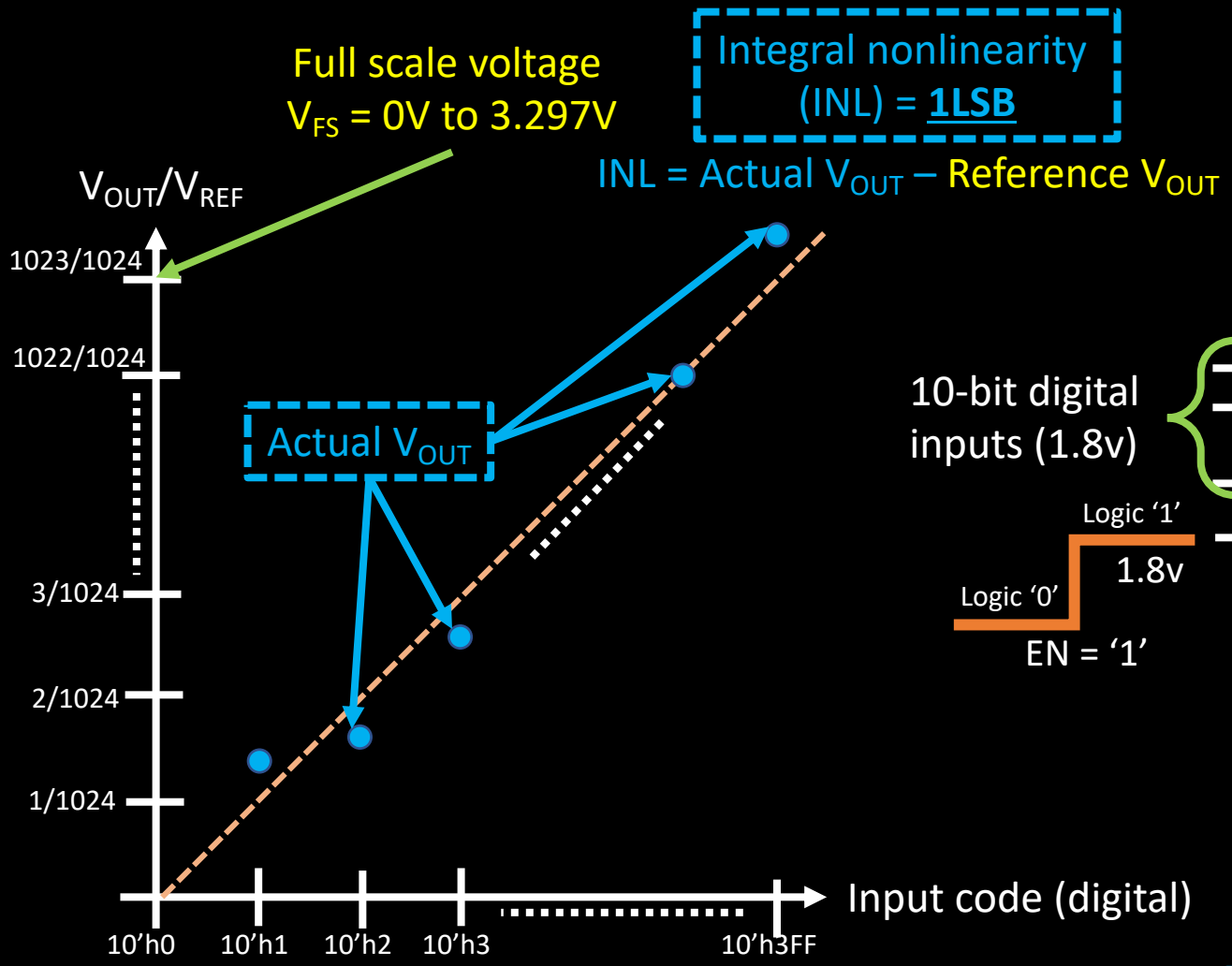


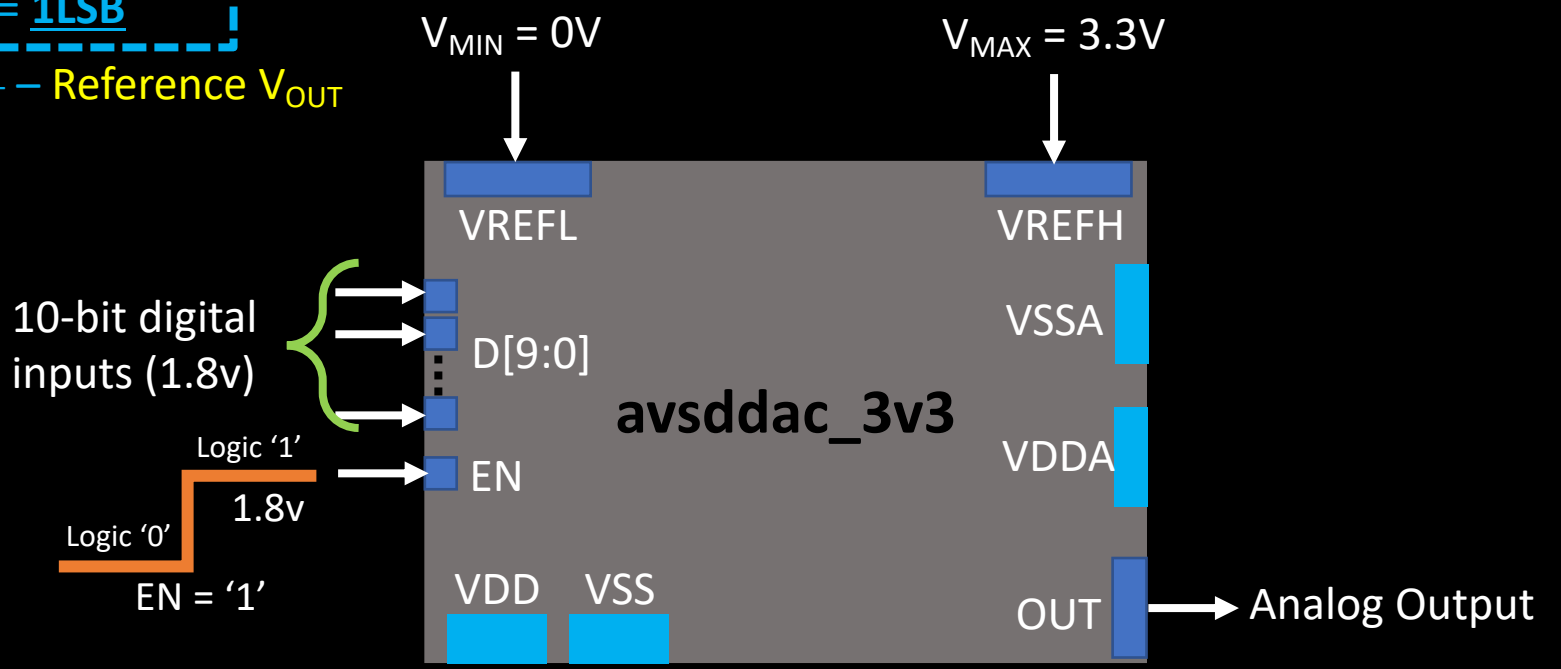
1LSB = 0.00322V or 3.2mV (1LSB = $V_{REF}/2^N$)
Resolution = 10bits (For V_{REF}=3.3V)

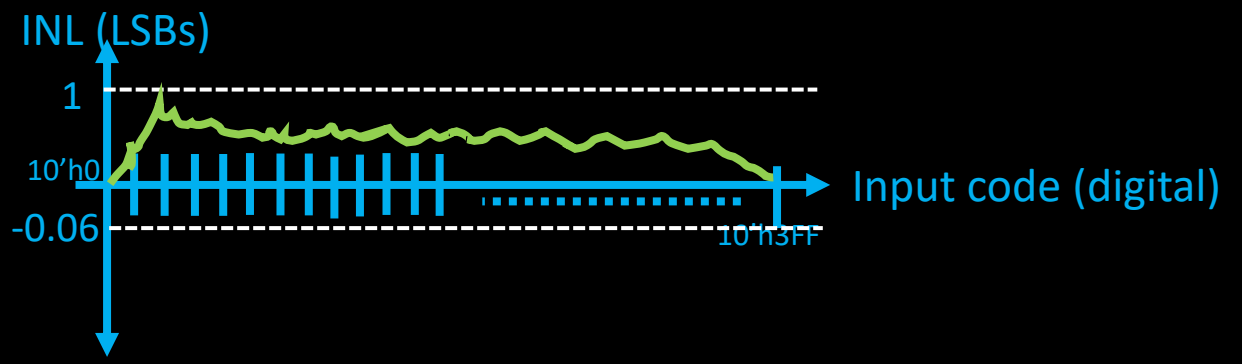
avsddac_3v3 operating modes



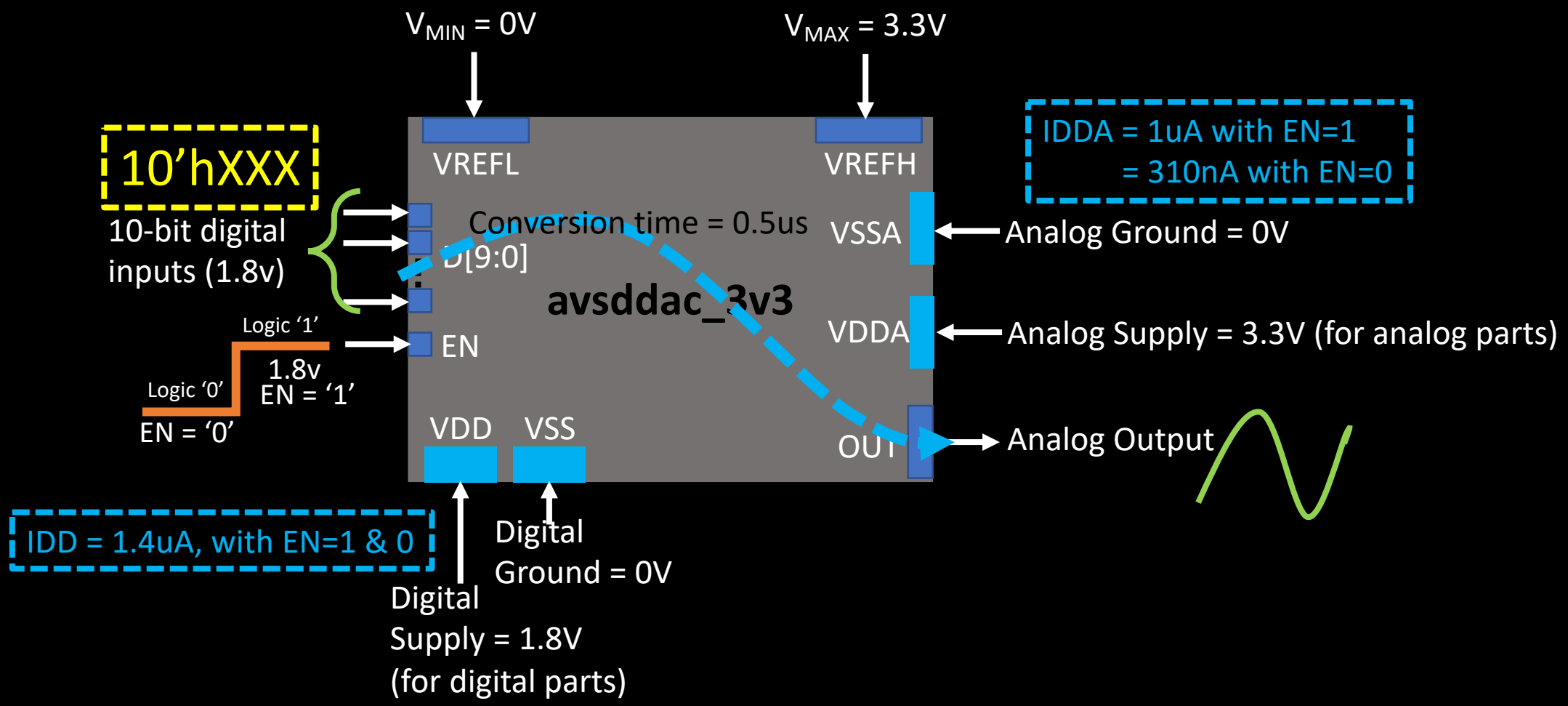
avsddac_3v3 operating modes







avsddac_3v3 operating modes



avsddac_3v3 plots and values needed

1) DNL vs Digital code at V_{REF}=V_{DD}=3.3V and T=20C & 85C
2) INL vs Digital code at V_{REF}=V_{DD}=3.3V and T=20C & 85C
3) DNL vs Digital code at V_{REF}= 1.25V, V_{DD}=3.3V and T=20C & 85C
4) INL vs Digital code at V_{REF}=1.25V, V_{DD}=3.3V and T=20C & 85C