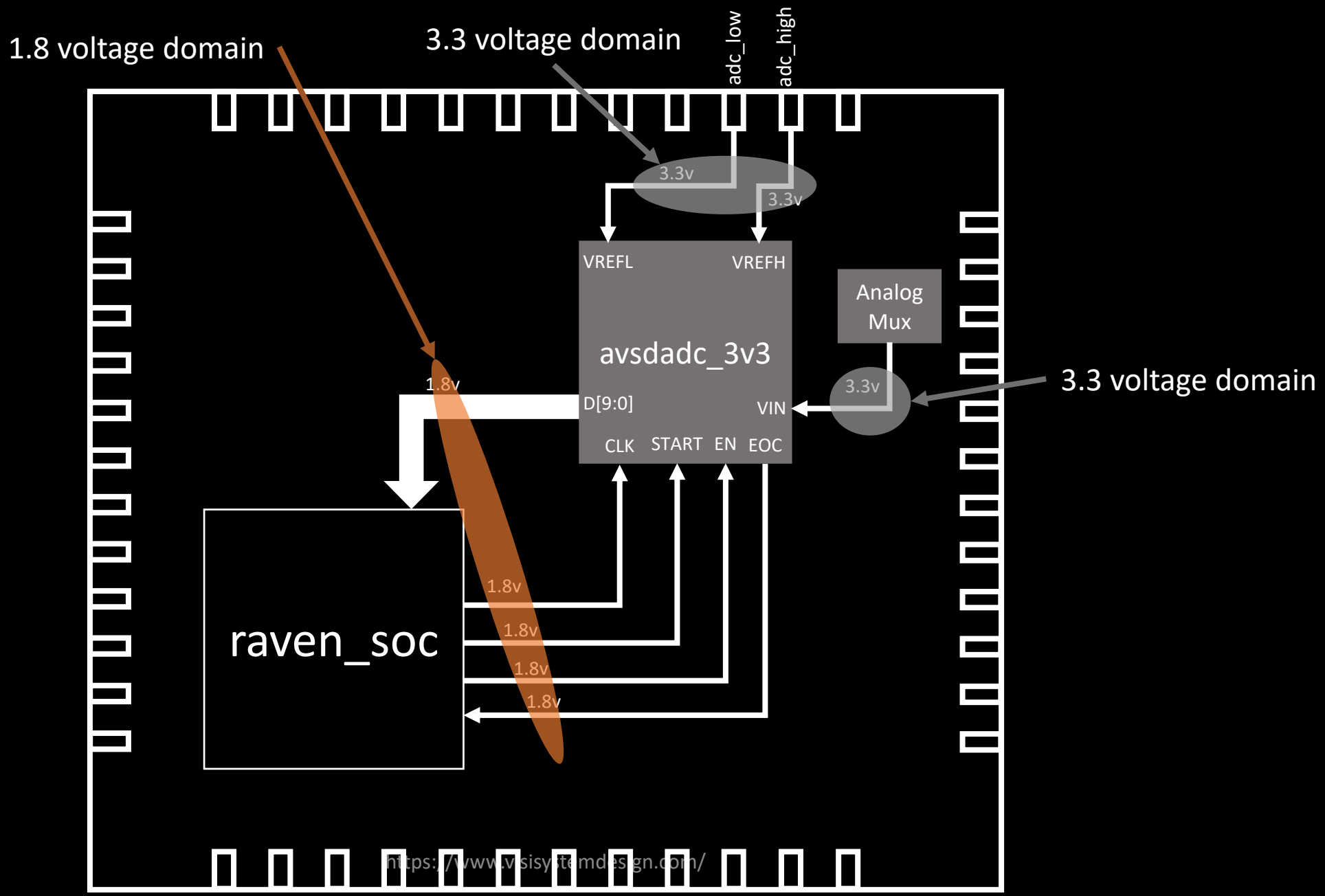
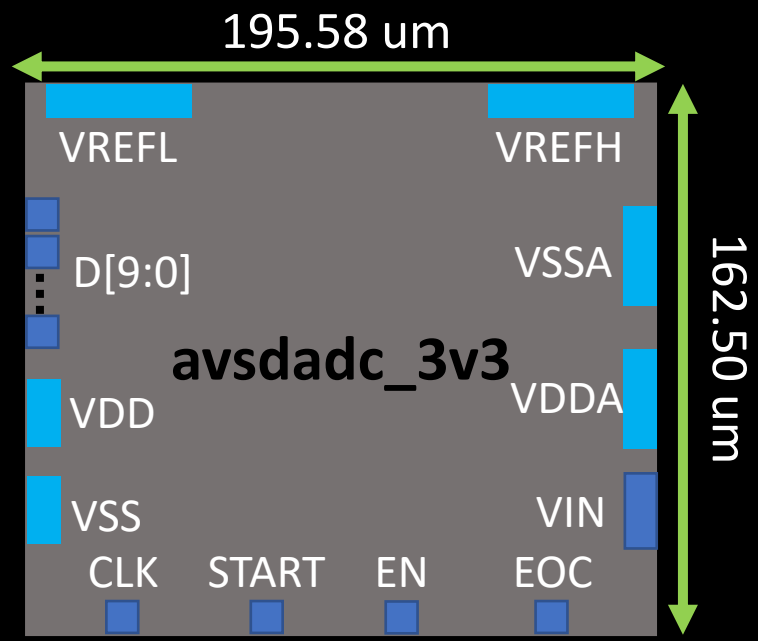
ADC (avsdadc_3v3) spec sheet for 180nm tech node

- Specs released under APACHE LICENSE 2.0
- Please contact Kunal at kunalpghosh@gmail.com in case of any doubts

Application Note for adc (avsdadc_3v3)



avsdadc_3v3 preferred dimensions, pin locations and metal layers



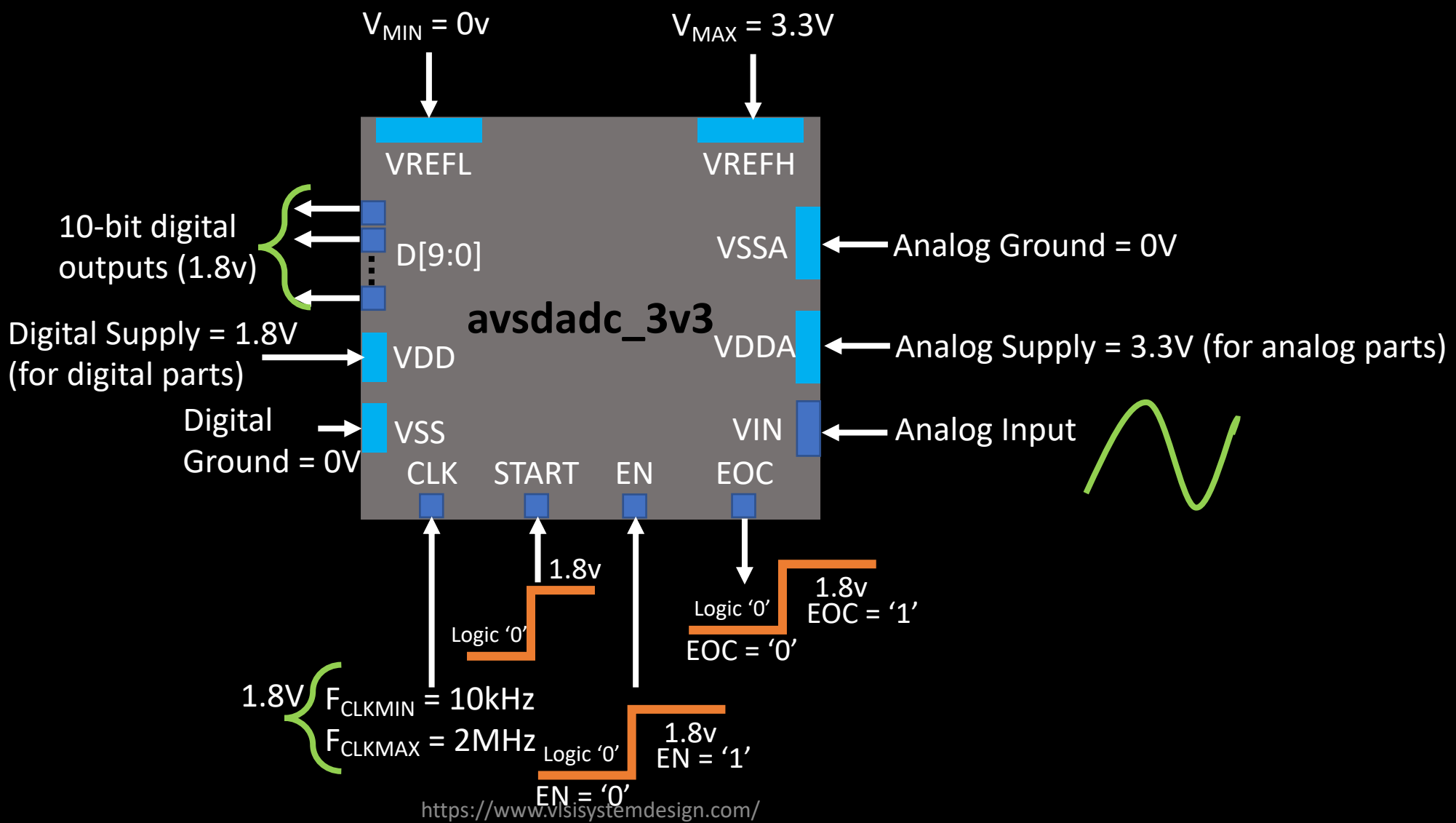
D[9-0], EN, EOC, CLK, START pins (metal3) – 0.28um x 0.28um

VDDA, VSSA pins (metal2) – 0.4um x 3um

VREFL, VREFH pins (metal2) – 9.48um x 0.4um

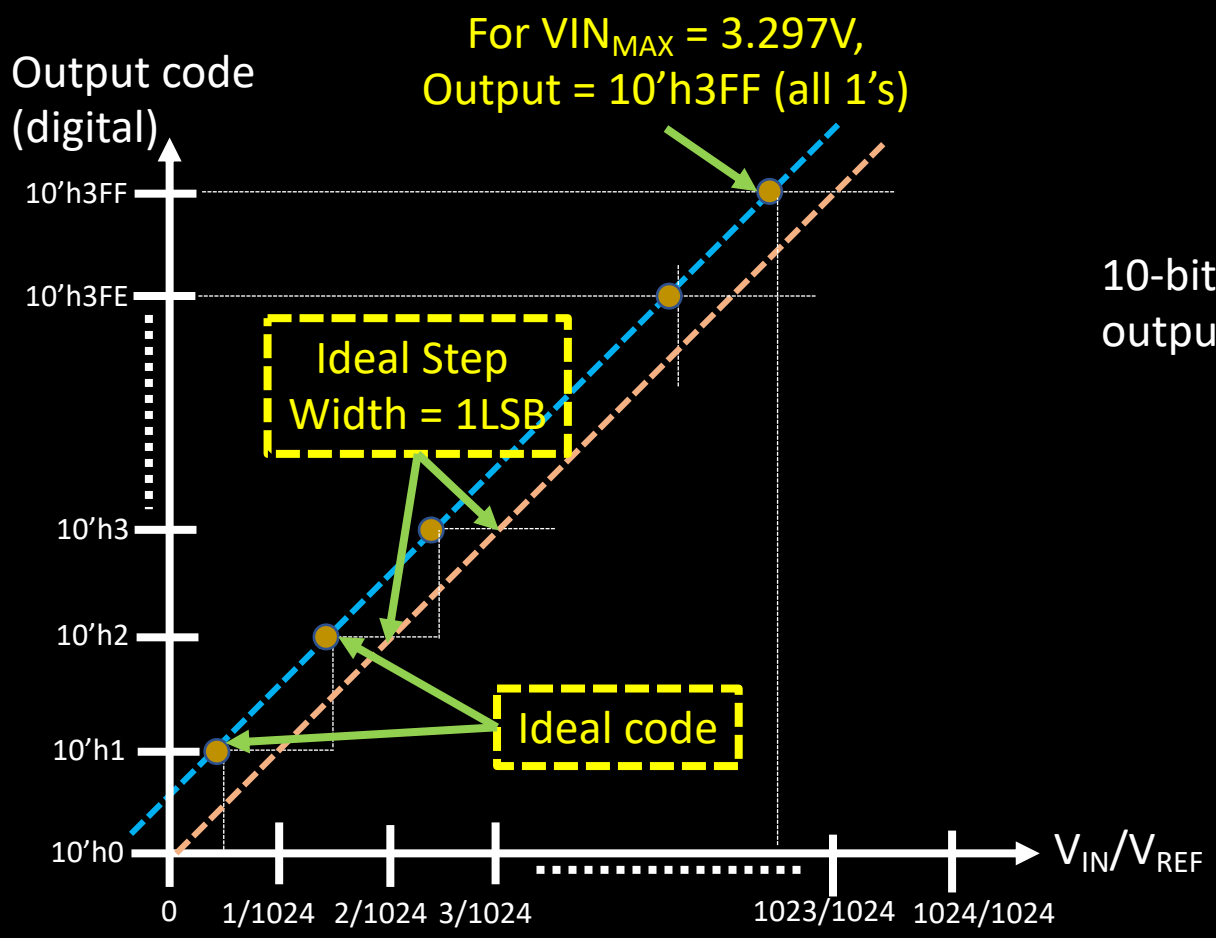
VDD, VSS pins (metal2) – 0.4um x 1.5um

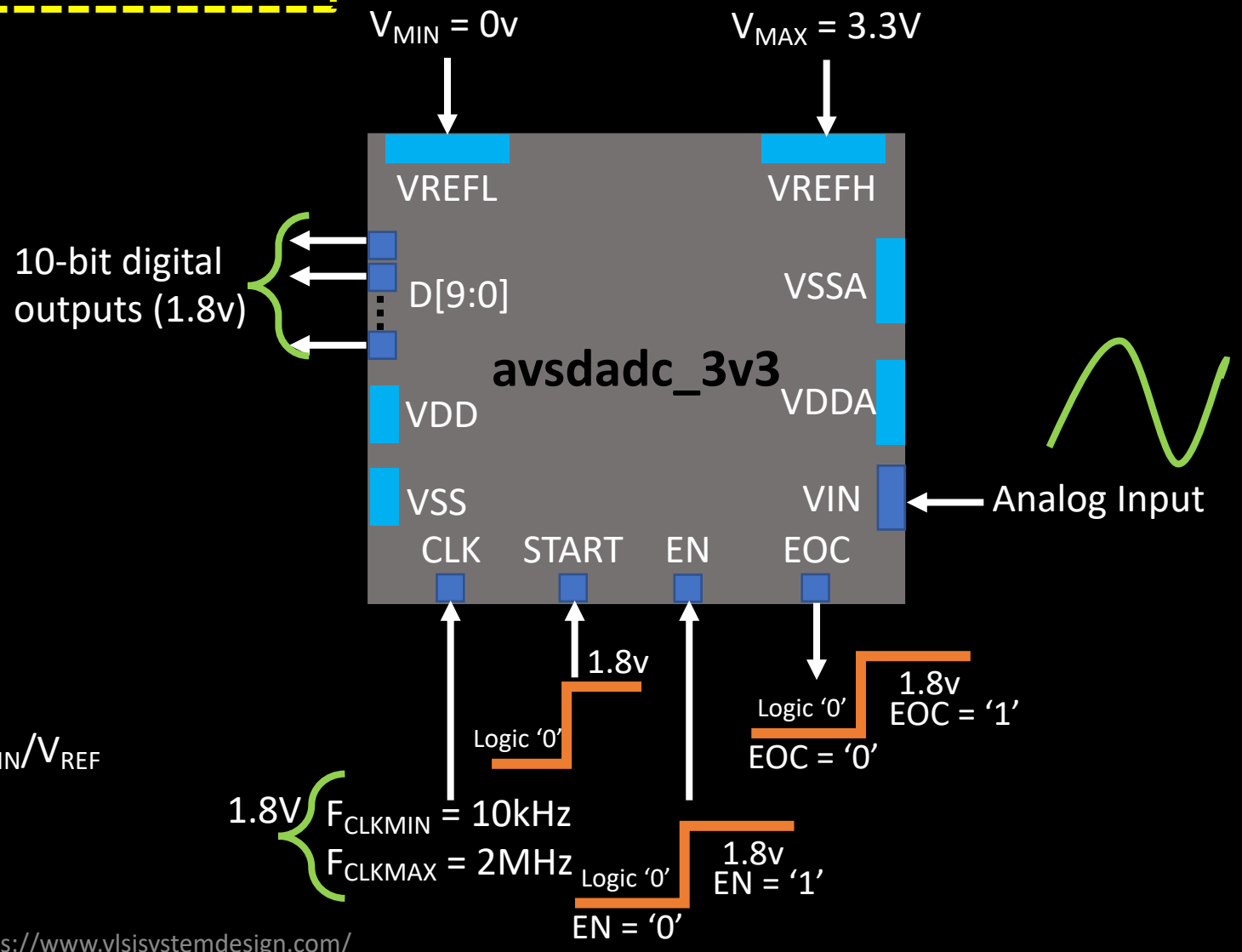
avsdadc_3v3 operating modes



avsdadc_3v3 operating modes (For F_{CLK}=1MHz)

1LSB = 0.00322V or 3.2mV (1LSB = $V_{REF}/2^N$)
Resolution = 10bits (For V_{REF}=3.3V)

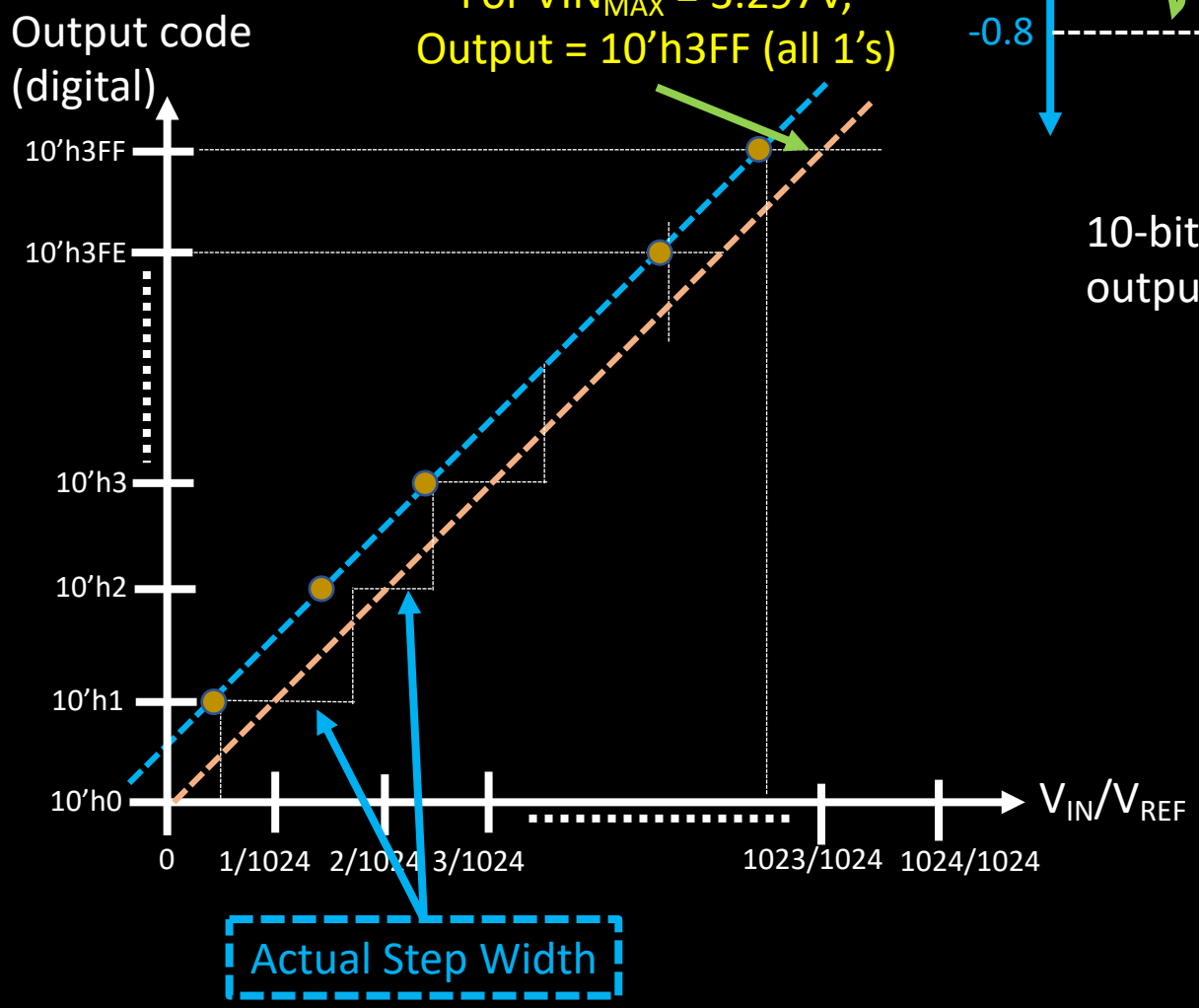


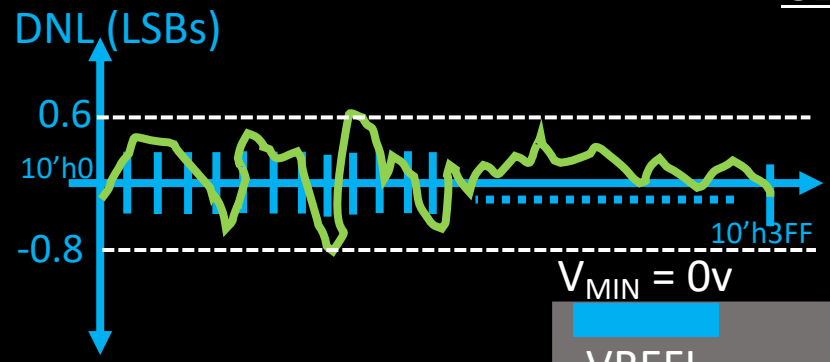


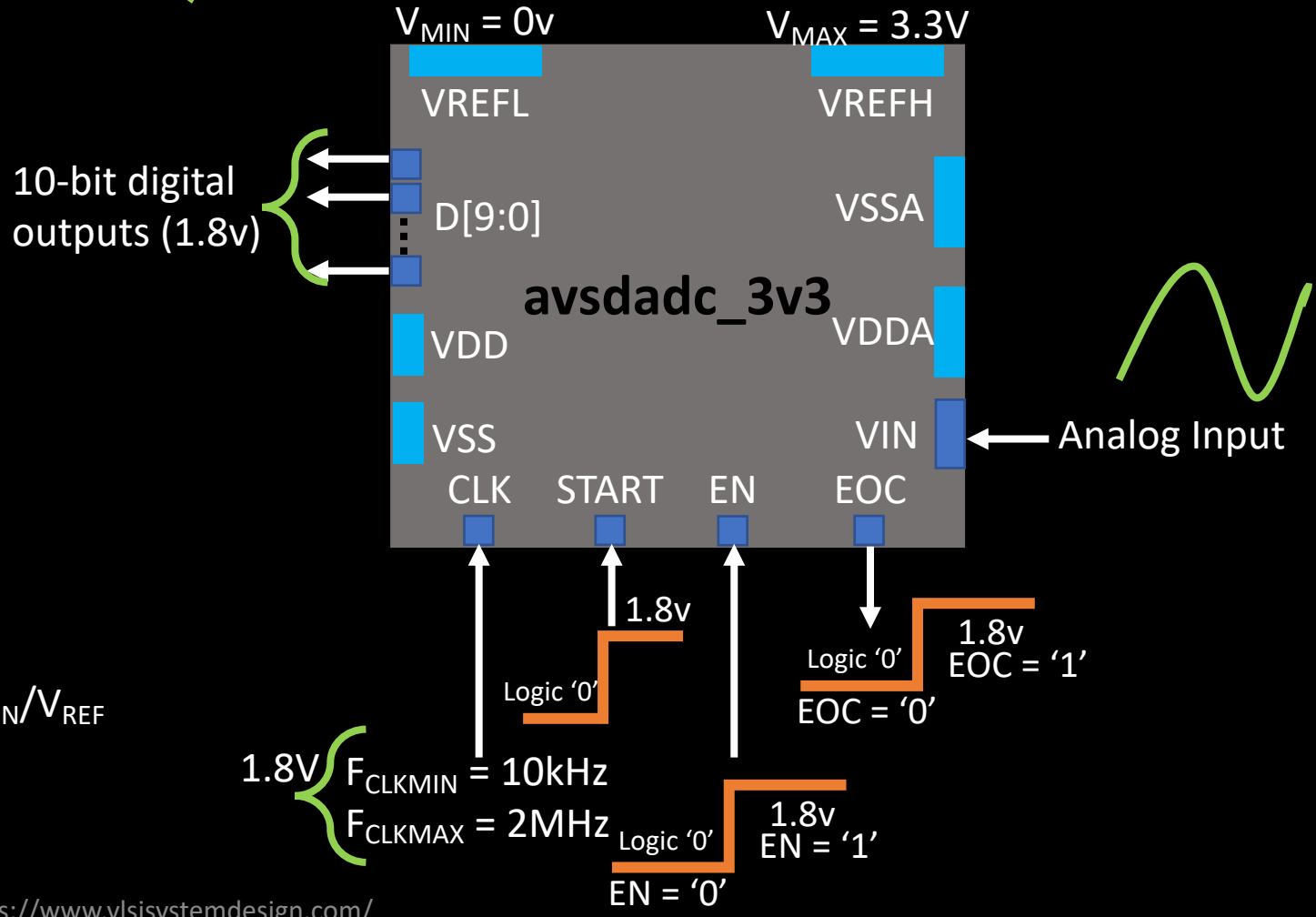
avsdadc_3v3 operating modes (For F_{CLK}=1MHz)

Differential nonlinearity (DNL) = **0. 8LSB**

DNL = Actual step width – Ideal step width



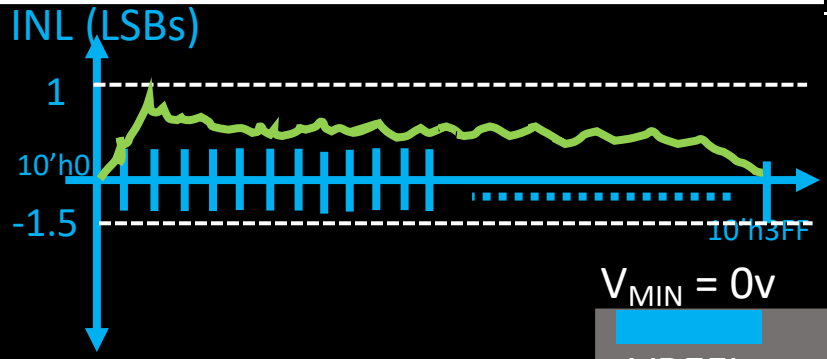




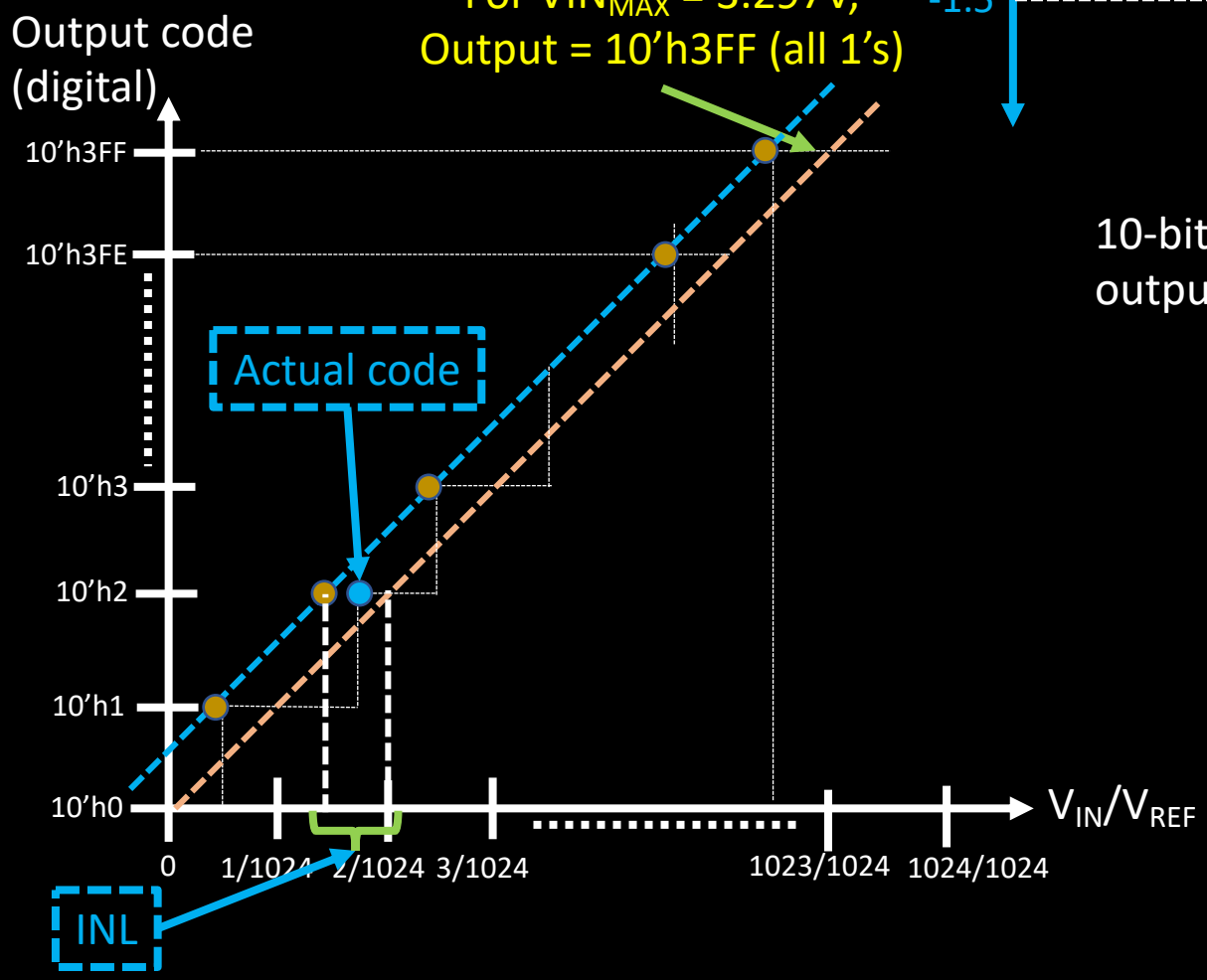
avsdadc_3v3 operating modes (For F_{CLK}=1MHz)

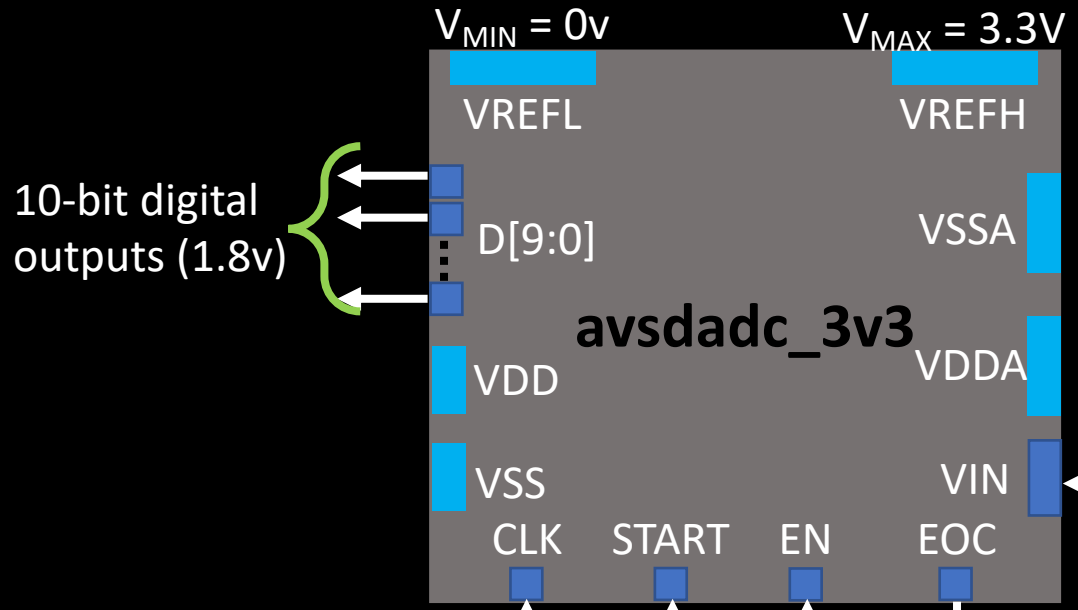
Integral nonlinearity (INL) = **1.5LSB**

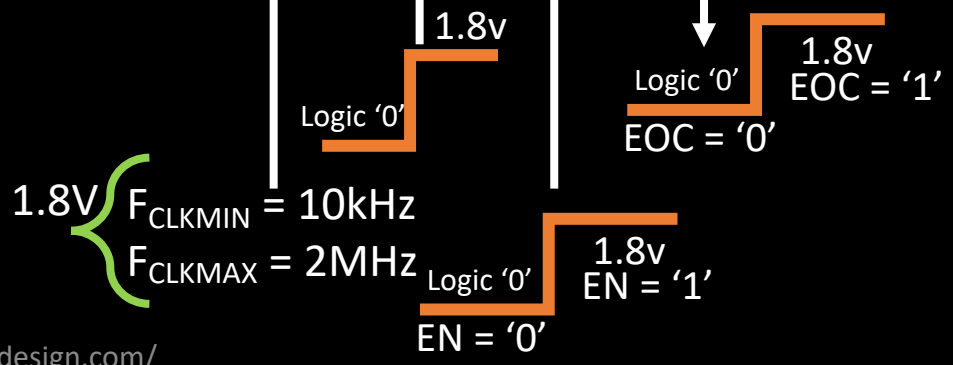
INL = Actual code – Reference code



For VIN_{MAX} = 3.297V,
Output = 10'h3FF (all 1's)

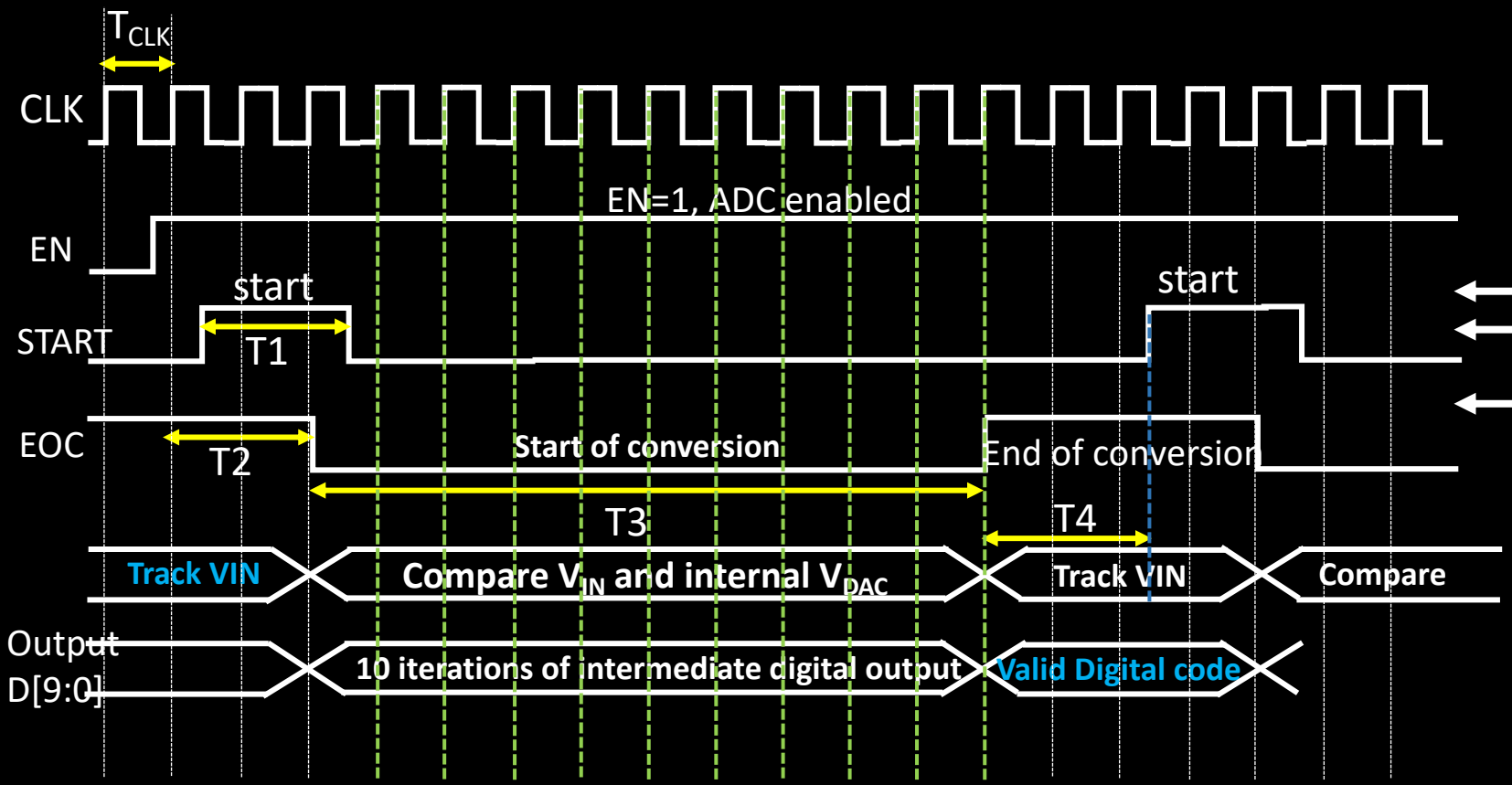


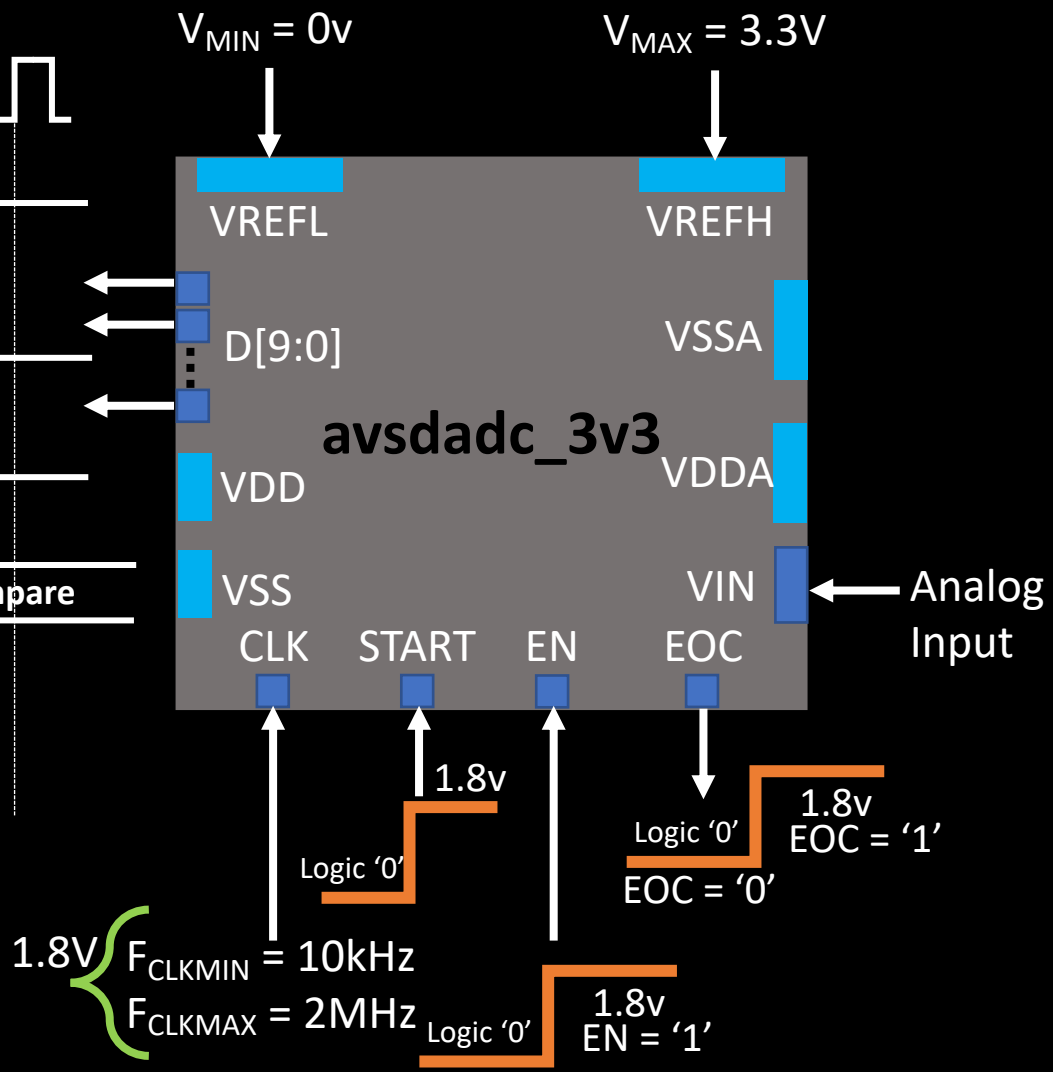




avsdadc_3v3 operating modes (For F_{CLK}=1MHz)

Total conversion time = SAR prep time (2 clock cycles) + Conversion time (10 clock cycles)





T1 = START signal duration min 2 clock cycles
T2 = SAR preparation time is up to 2 clock cycles
T3 = Conversion time is 10 clock cycles
T4 = At least 1us needed to track V_{IN}

avsdadc_3v3 plots and values needed

1) DNL vs Digital code at V_{REF}=V_{DD}=3.3V; F_{CLK}=2MHz and T=20C
2) INL vs Digital code at V_{REF}=V_{DD}=3.3V; F_{CLK}=2MHz and T=20C
3) DNL vs Digital code at V_{REF}= 1.25V, V_{DD}=3.3V; F_{CLK}=2MHz & 1MHz and T=20C
4) INL vs Digital code at V_{REF}=1.25V, V_{DD}=3.3V; F_{CLK}=2MHz & 1MHz and T=20C