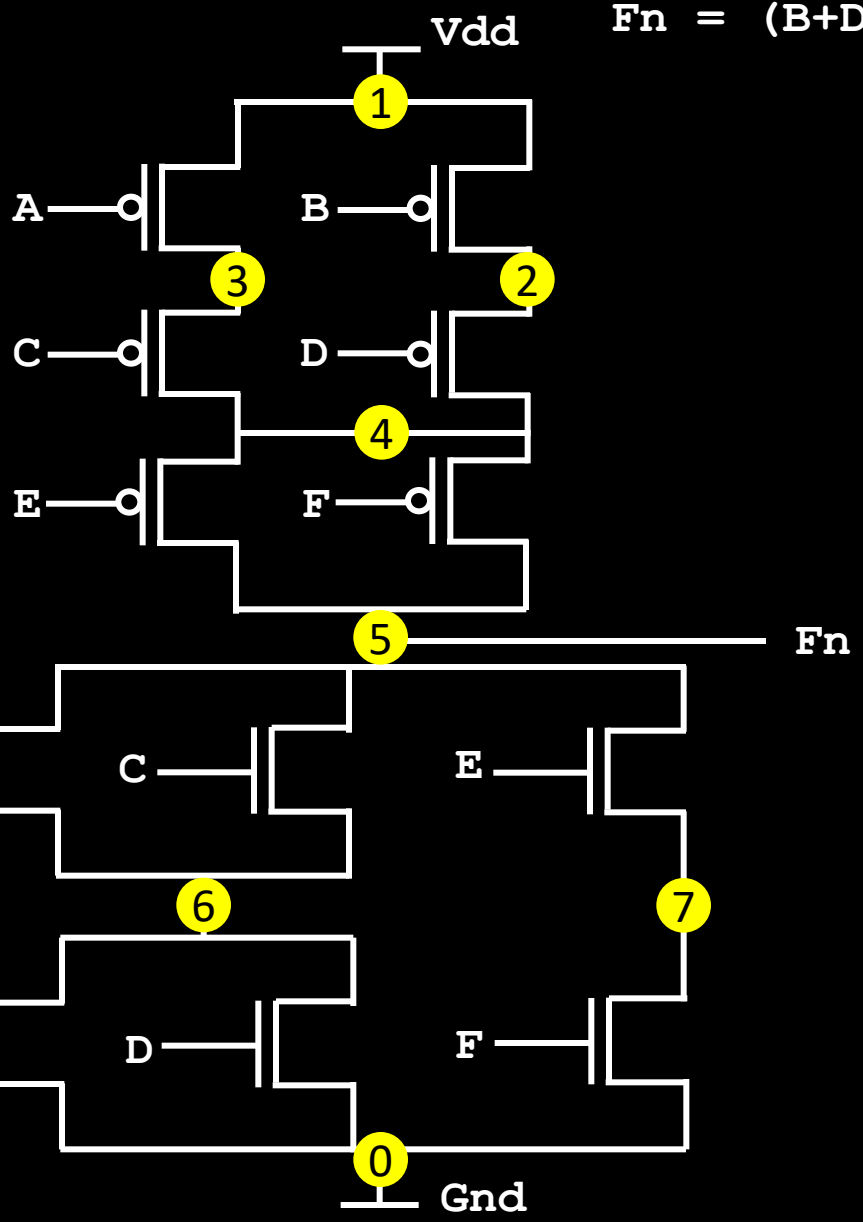
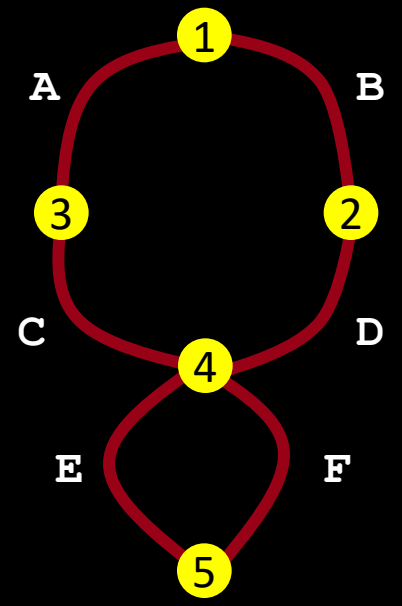
A tool to automatically convert
any analog circuit spice netlist to its equivalent layout

- **Specs released under APACHE LICENSE 2.0**
- **Please contact Kunal at kunalpghosh@gmail.com in case of any doubts**

Art of layout – Euler's path and stick diagram

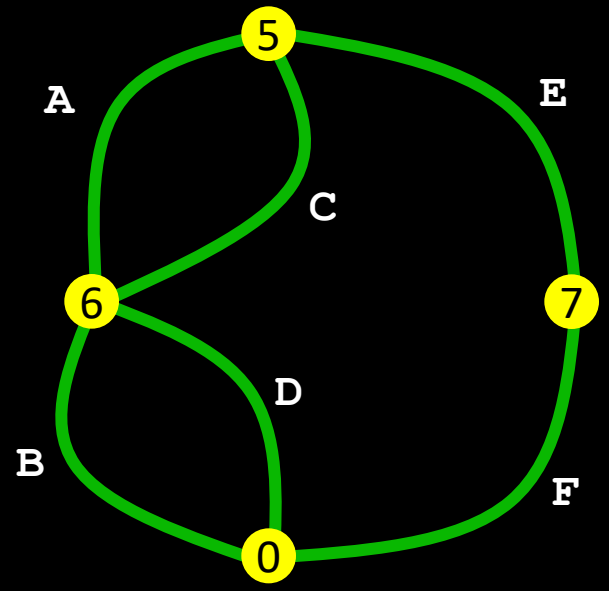
$$Fn = \overline{(B+D).(A+C)+E.F}$$





pmos network graph

nmos network graph



Art of layout – Euler's path and stick diagram

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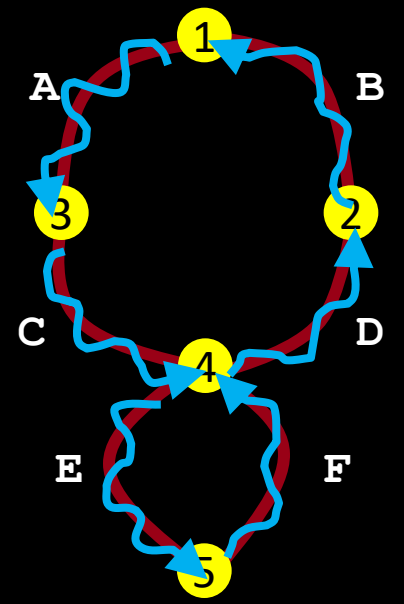
A – C – E – F – D – B



pmos network graph

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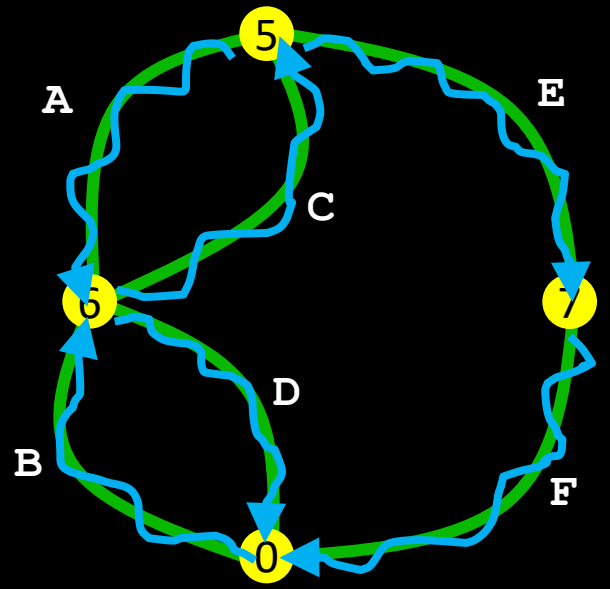

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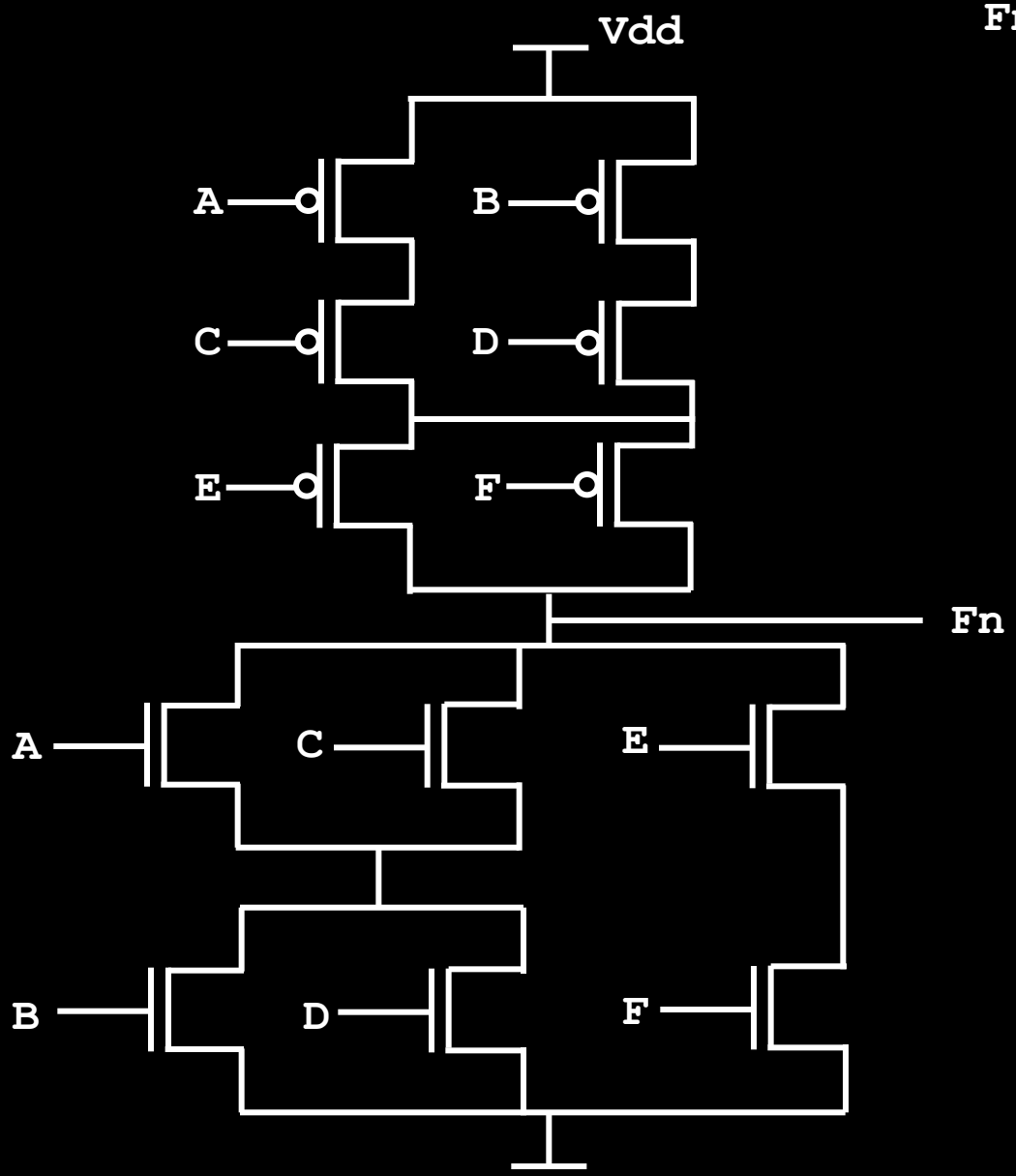
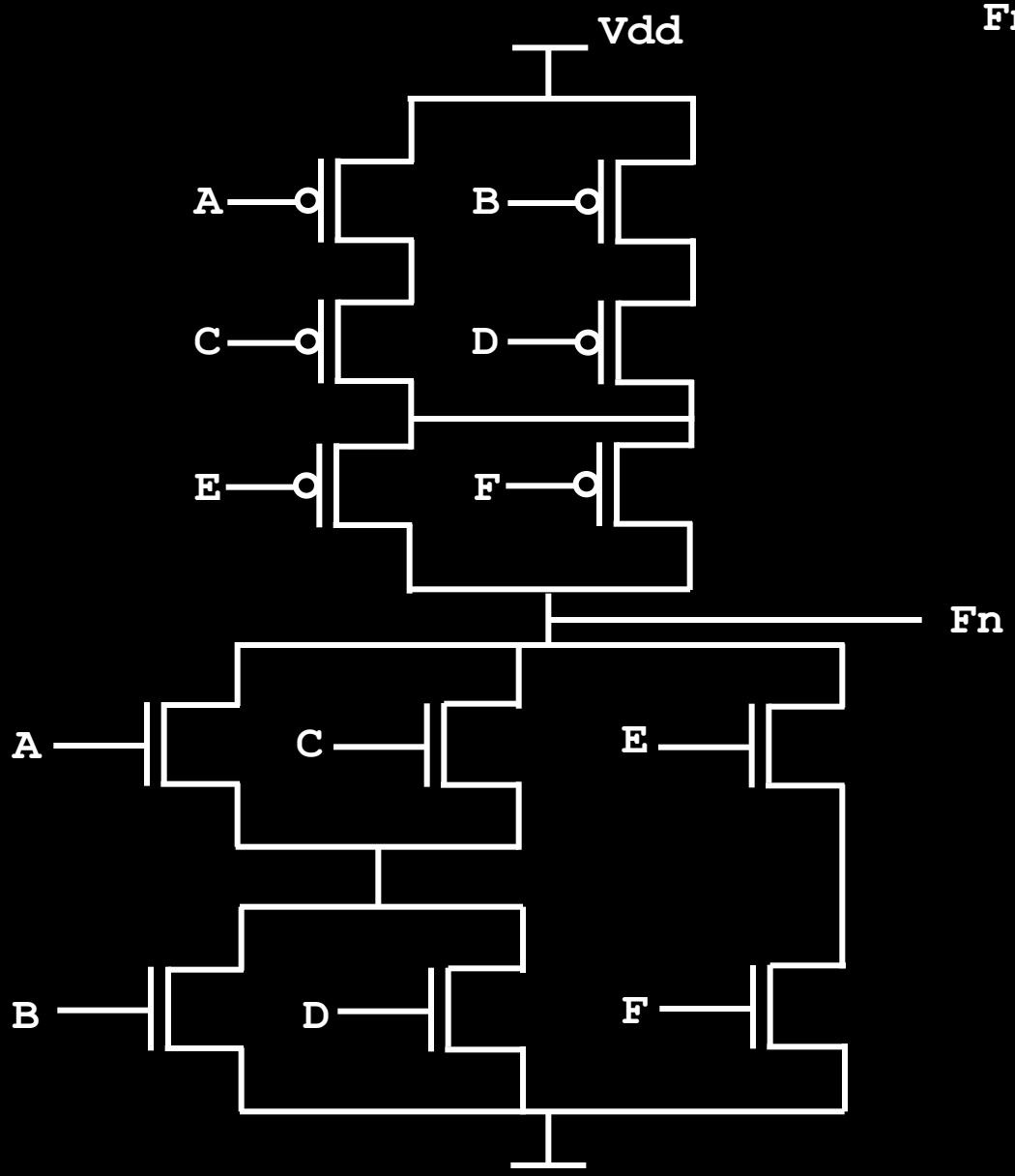
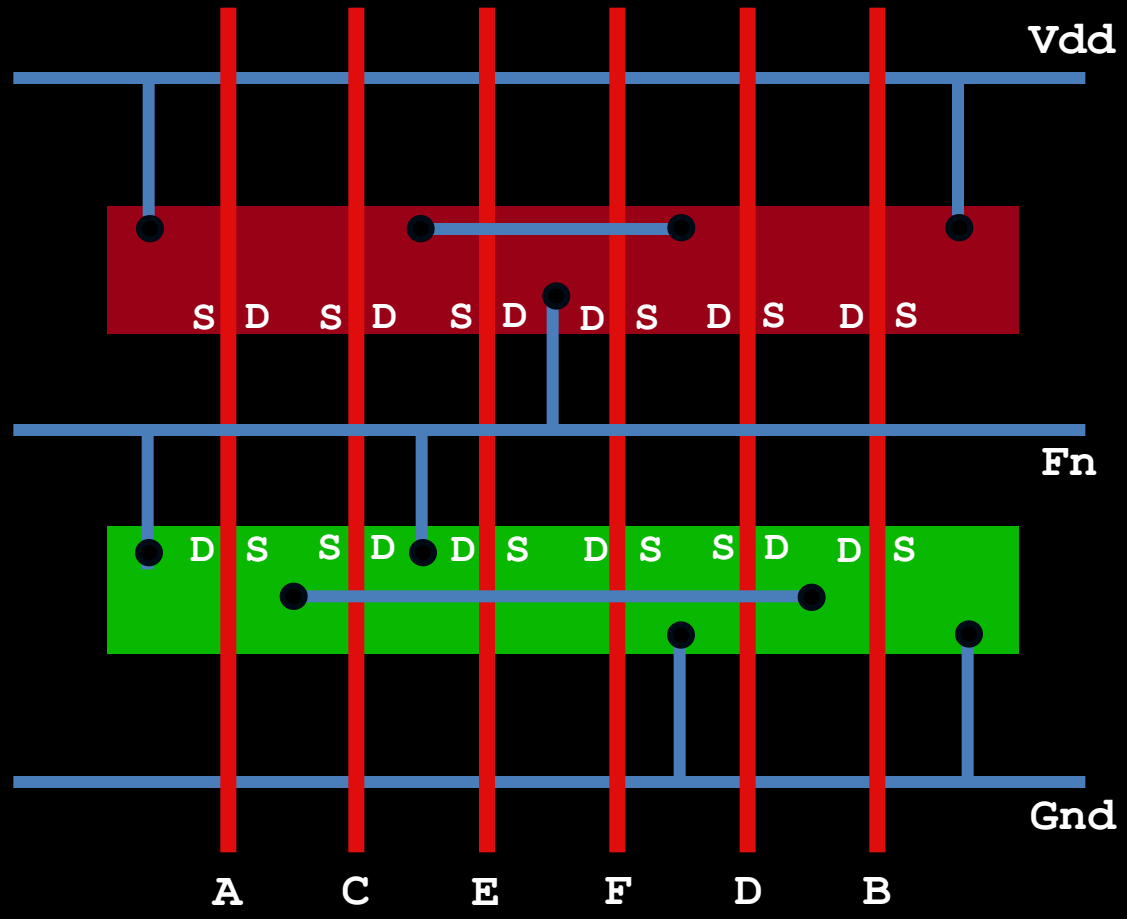


Art of layout – Euler's path and stick diagram

$$Fn = \overline{(B+D).(A+C)+E.F}$$

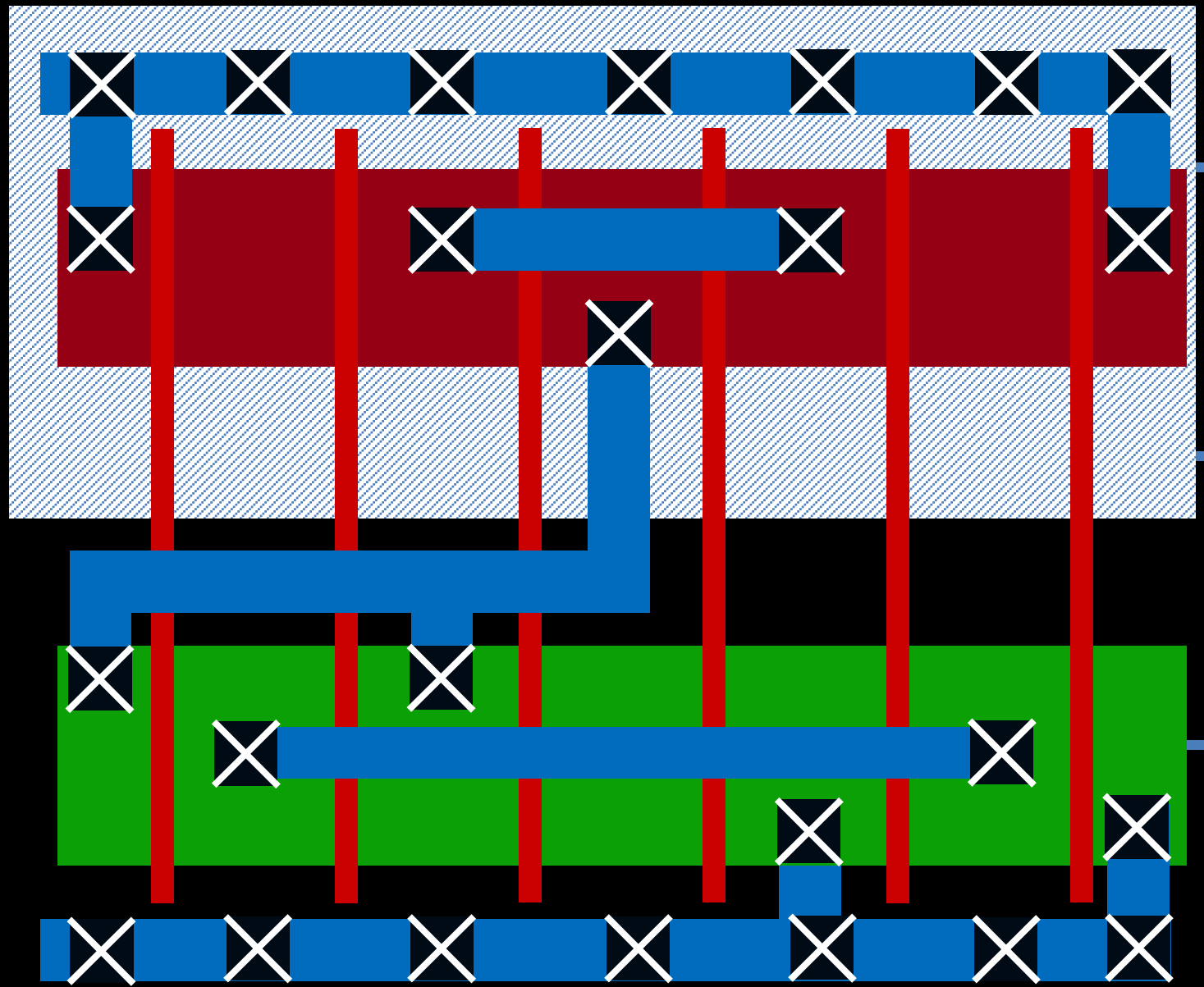


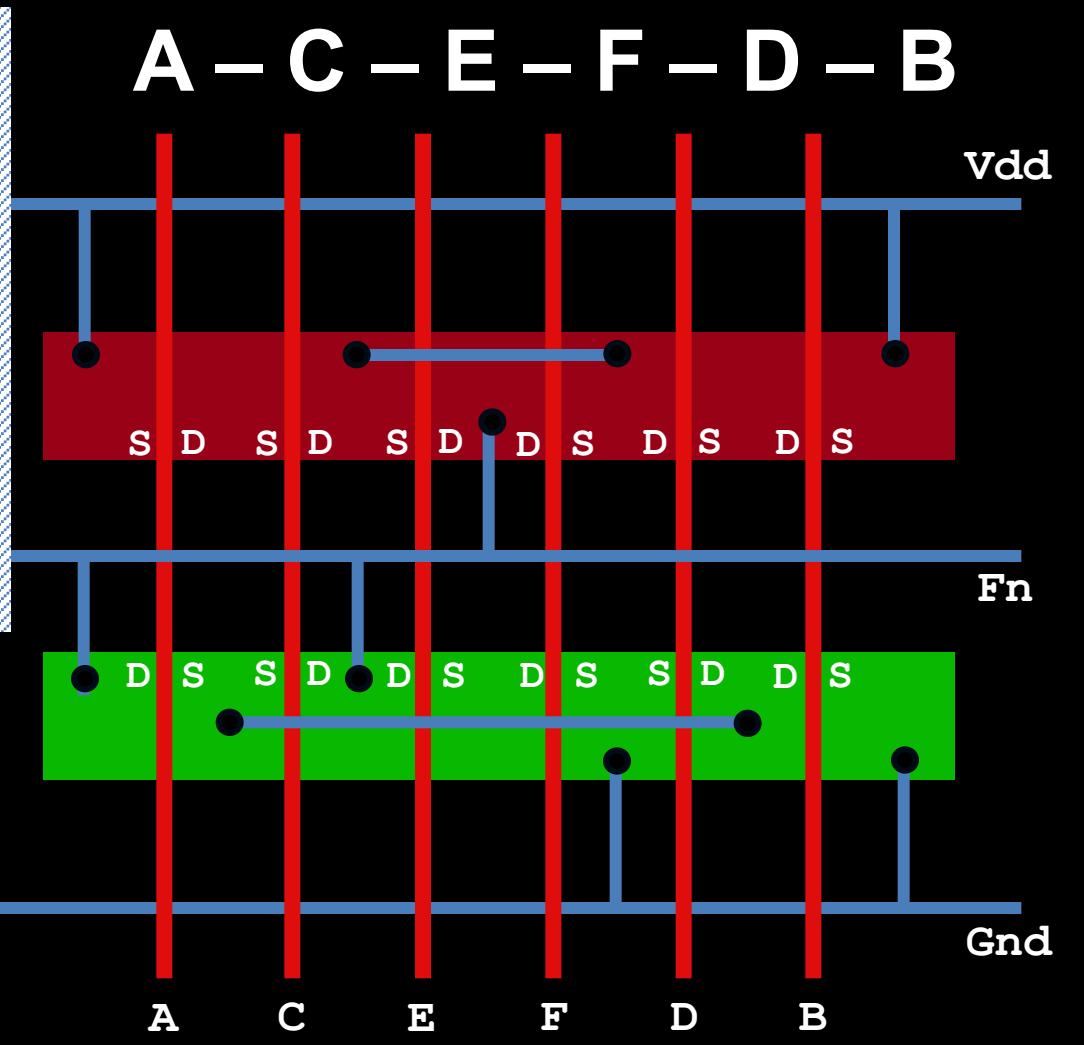
A – C – E – F – D – B



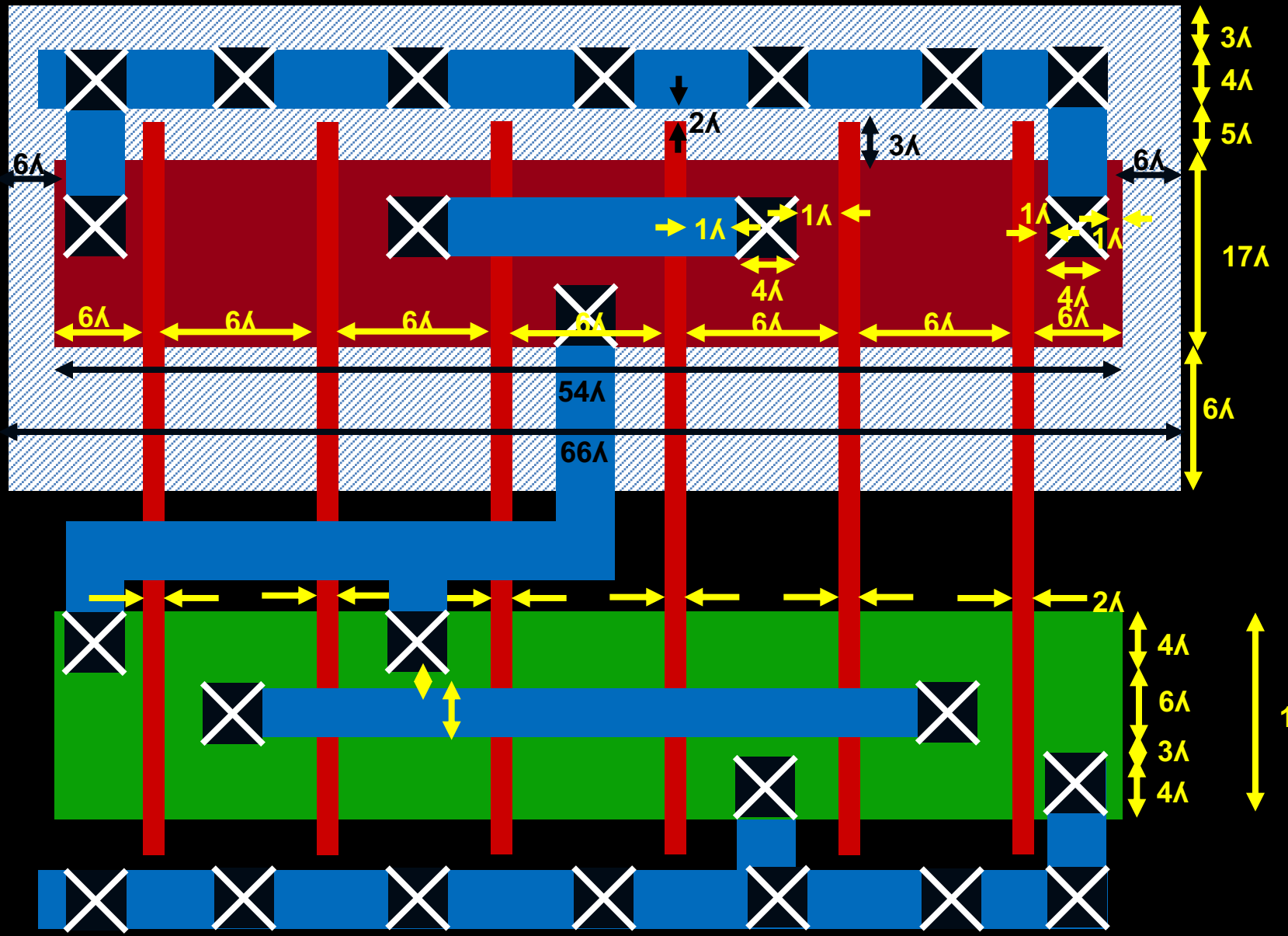
Art of layout – Euler's path and stick diagram

$$Fn = (B+D).(A+C)+E.F$$



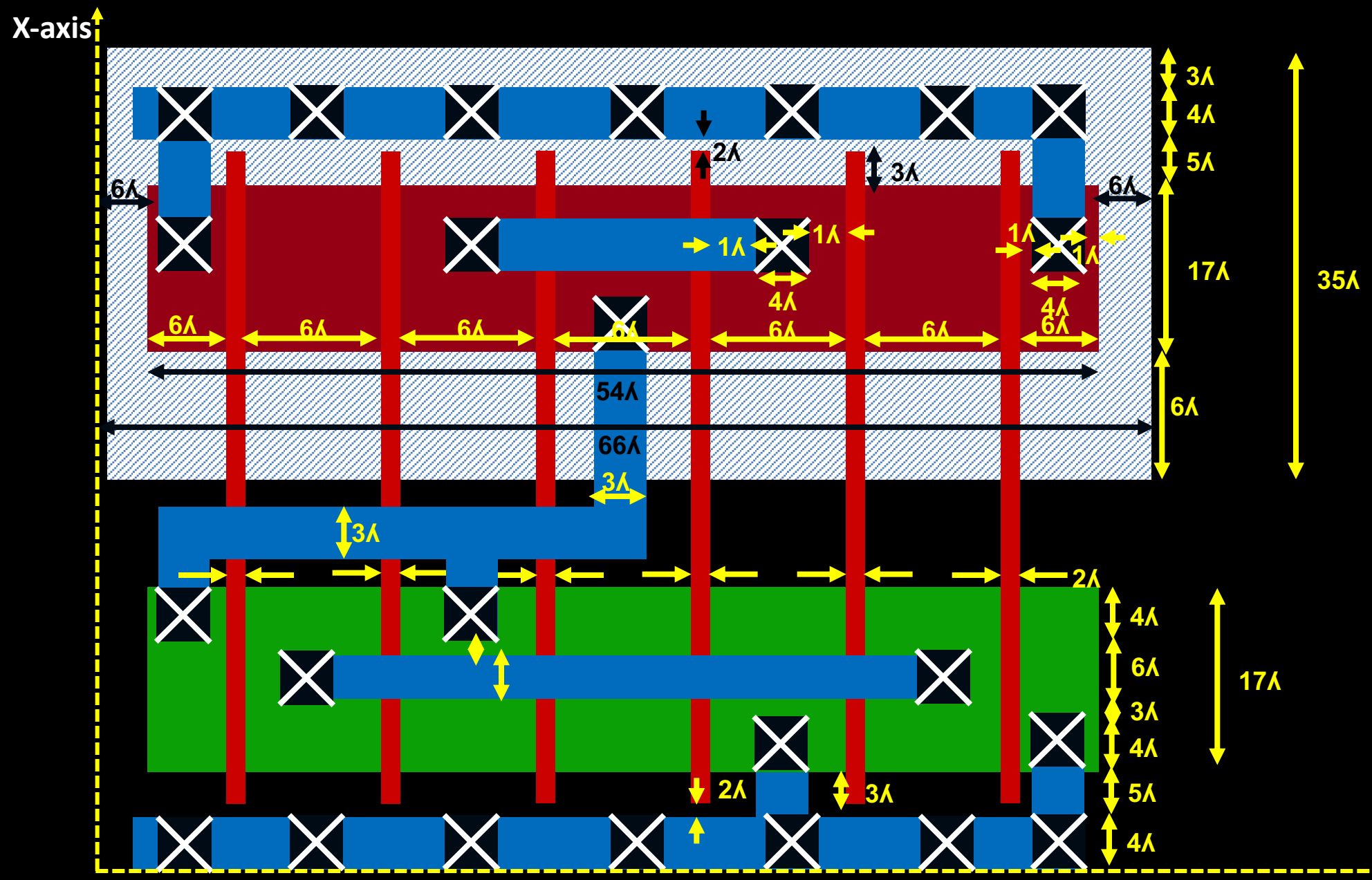


Art of layout – Euler's path and stick diagram + A – C – E – F – D – B



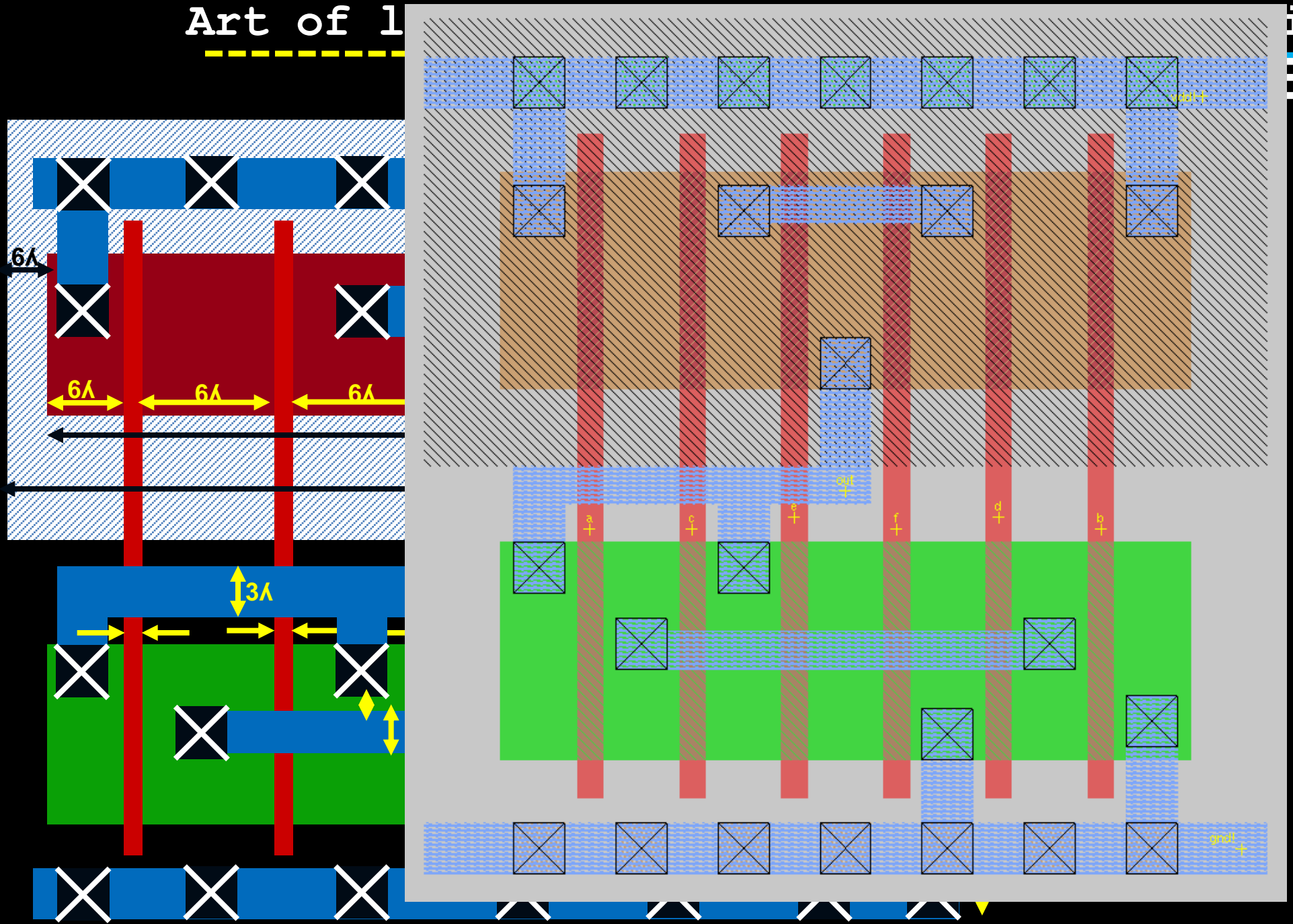
details (min)	Design rule
poly width	2λ
extension over active	3λ
poly to active spacing	1λ
poly to ndc spacing	1λ
ndc width	4λ
metal width	3λ
poly to metal spacing	n/a
ndc to ndc spacing	2λ
active/diffusion width	3λ

Art of layout – Euler's path and stick diagram

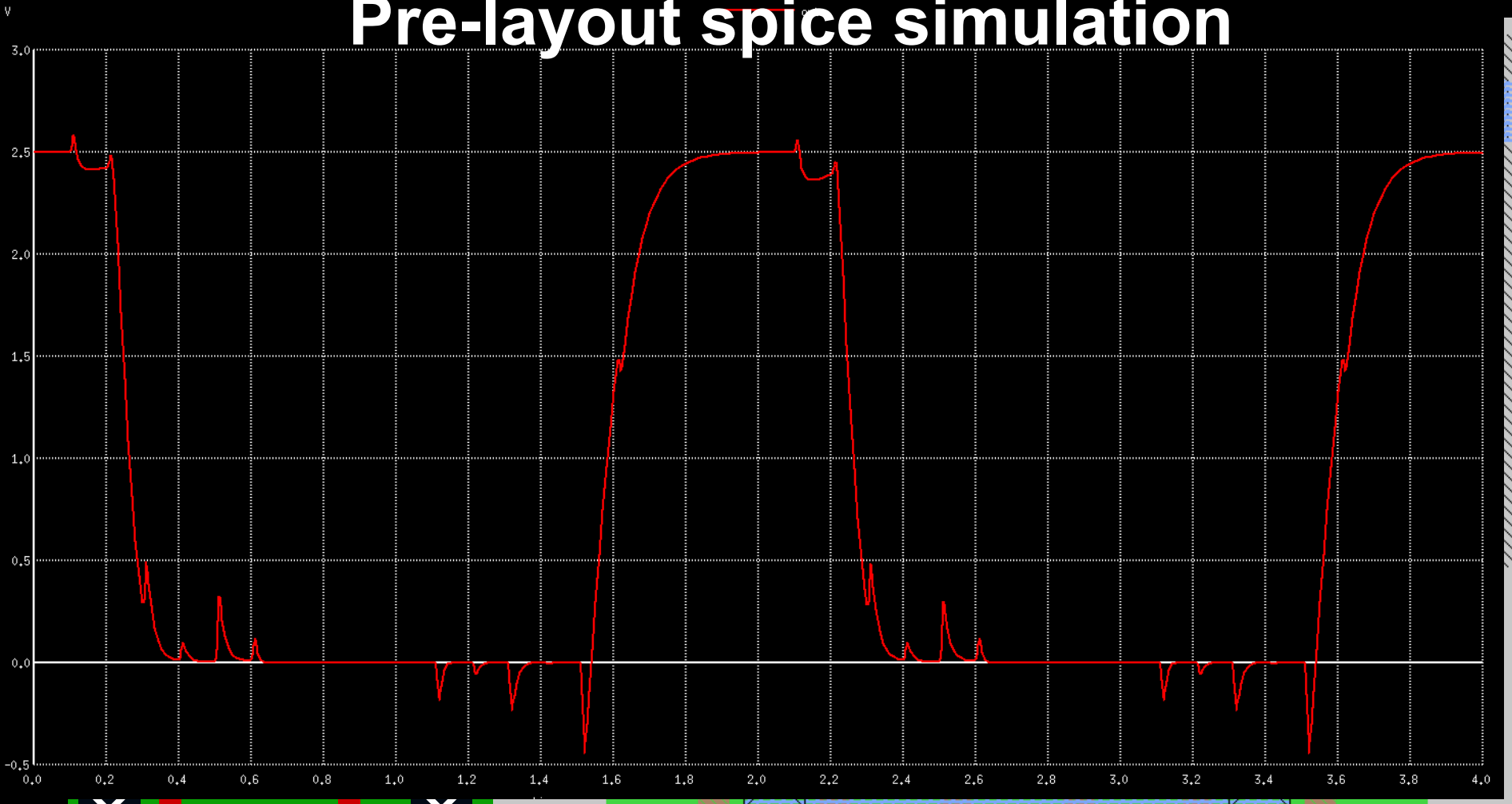


Art of l iagram

E – F – D – B

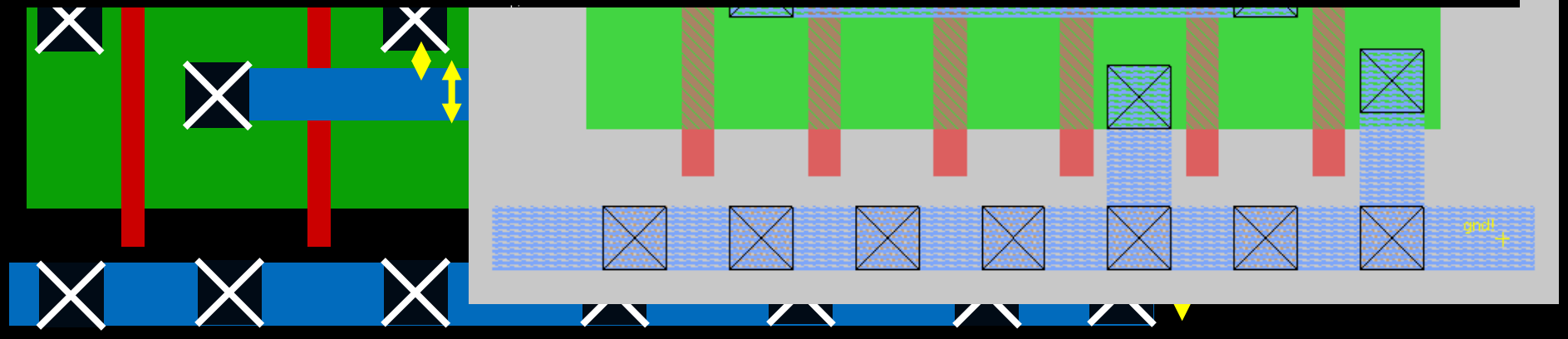


Pre-layout spice simulation

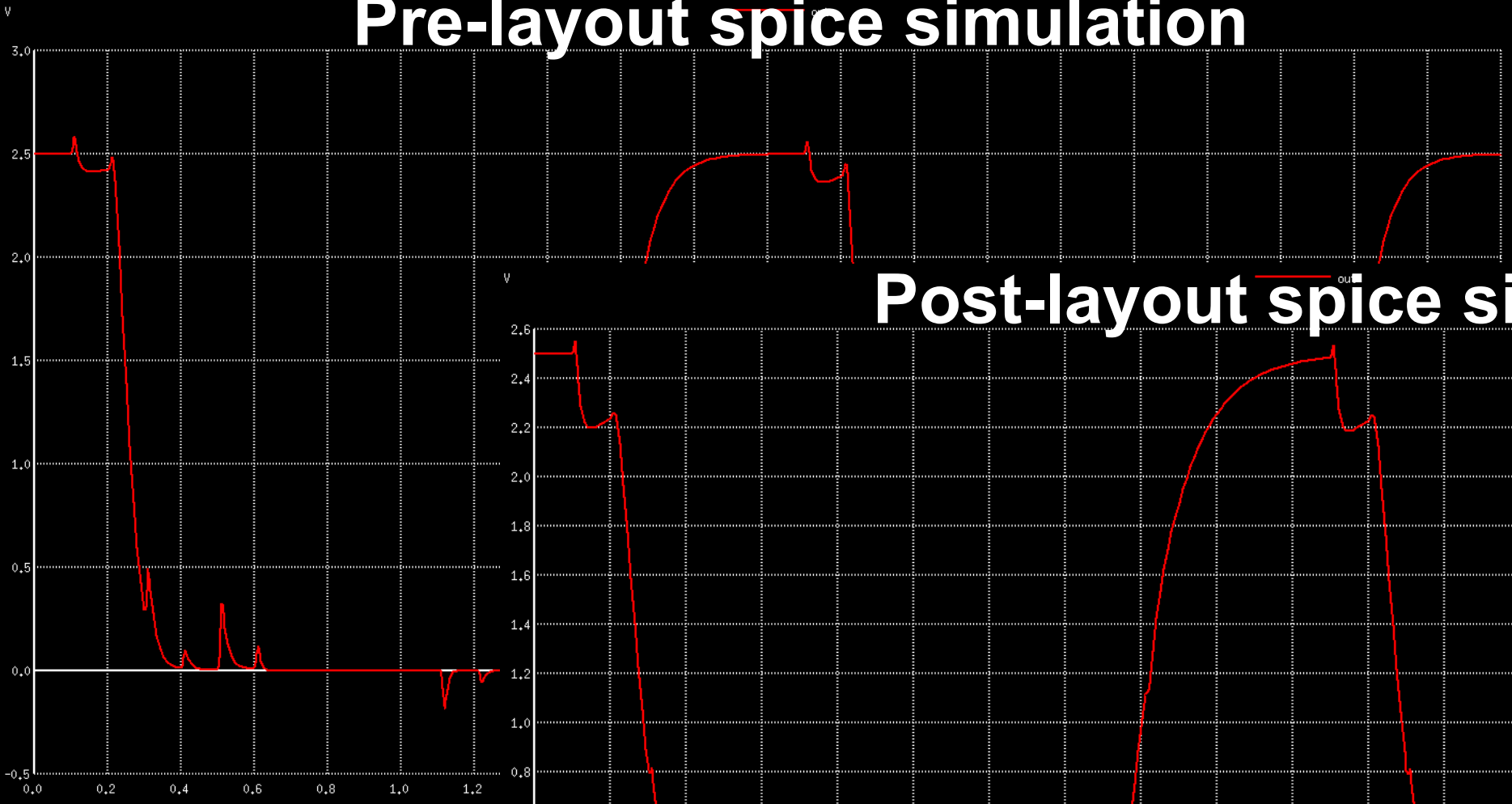


iagram

E – F – D – B



Pre-layout spice simulation



Post-layout spice simulation