



The synthesized netlist is given to PNR tool (Qflow) and finally Sign-off is done with STA tool (using Opentimer). The output of the flow is GDSII layout and performance & area metrics of your design. VSDFLOW also provide hooks at all stages for users working at different levels of design flow. It is tested for 30k instance count design like ARM Cortex-M0, RISC-V picorv32, and can be further tested for multi-million instance count using hierarchical or glue logic.

Its updated and now available for download for FREE...Here's the link:

<https://github.com/kunalg123/vsdflow>

VSD Proprietary