Electronics & ICT Academy

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WORKSHOP
ON
"DEVICE MODELING USING SYNOPSYS SENTAURUS"

(Date: 16-20 September, 2019)

Venue: NIT Manipur

Reporting Time on 16 Sept, 2019	:	**9:00 AM**
Course Duration on 17 – 20 Sept, 2019	:	**9:30 AM – 5.30 PM**
Morning Tea Break	:	**11:00AM – 11.10AM**
Lunch Break	:	**1:00 PM – 1:40 PM**
Evening Tea Break	:	**03:30PM – 3:40PM**

Day 1(16 – 09 – 19)

Aim: To study the importance of MOSFET device and understand TCAD flow to model MOSFET using sprocess, sdevice and svisual (**Theory** – 4 hours, **Lab** – 3 hours)

- Chip design flow overview
- Impact of device modelling on entire chip design flow
- How to characterize inverter delay and butterfly curve using ngSPICE?
- Introduction to generic TCAD flow using sprocess, sdevice and svisual

Day 2 (17 – 09 – 19)

Aim: NMOS Drain current modelling, SPICE simulations and Introduction to 16-Mask CMOS process (**Theory** – 3 hours, **Lab** – 4 hours)

- Strong inversion, threshold voltage with and without substrate potential
- NMOS resistive and saturation region of operation
- Velocity saturation drain current model
- 16-Mask process CMOS technology

Day 3 (18 – 09 – 19)

Aim: NMOS device modelling using sprocess, characterization using sdevice and analysis using svisual (**Theory** – 3 hours, **Lab** – 4 hours)

- Pao/Sah's Double integral and charge sheet model
- Introduction to 'sprocess' and 'sdevice' command files for NMOS

- Analyze drain current and MOS Capacitance plots using 'svisual'

Day 4 (19 – 09 – 19)

Aim: PMOS drain current modelling, PMOS device modelling using sprocess, characterization using sdevice and analysis using svisual (**Theory** – 2 hour, **Lab** – 5 hours)

- Introduction to PMOS device and its drain current
- Introduction to 'sprocess' and 'sdevice' command files for PMOS
- Analyze drain current and MOS Capacitance plots using 'svisual'

Day 5 (19 – 09 – 19)

Aim: NMOS/PMOS device BSIM model extraction using sdevice/svisual and "butterfly" curve analysis (**Theory** - 4 hours, **Lab** – 3 hours)

- Steps to extract BSIM models for NMOS and PMOS
- Introduction to standard SRAM butterfly curve
- Plug above NMOS/PMOS extracted BSIM models to generate butterfly curve and analyze performance using ngspice
- Fine tune device parameters, redo NMOS/PMOS device modelling using TCAD flow and reanalyze butterfly curve using new extracted BSIM models