Summer FDP on "VLSI Chip Design Hands on using Open Source EDA" (08 – 12 July, 2019)

Jointly organized by: Electronics & ICT Academies at- IIT Guwahati, IIITDM Jabalpur, MNIT Jaipur, NIT Patna, IIT Roorkee and NIT Warangal.

Module	Lecture/Invited Talk	Topics	Speakers
Module 01 ***SoC Planning***	**Invited Talk 1**	A short talk on Open Source tools and their usage in the VLSI Design (especially MAGIC will be covered)	**Dr. Anand Bulusu** **(IIT Roorkee)**
	Interactive Lecture 1	**SoC Design (RISC-V SoC, which implements RISC-V IMC ISA) – (Theory) :** • RISC-V and picoSoC overview • Overview about SoC planning, like placing pads, macros, memories and IP's • Overview about design cycle, like RTL synthesis, physical design, layout, DRC, clock tree synthesis and STA.	**Mr. Kunal P Ghosh** **(Director, VSD Corp. Pvt. Ltd.)**
Module 02 ***Floor planning & timing analysis***	**Interactive Lecture 2**	**Pre-layout timing analysis (Lab - OpenSTA) and Floorplanning (Lab – MAGIC):** • Setup/Hold analysis **(Theory + Labs)** • Report nworst, timing_qor, analysis_coverage in clock ideal mode **(Theory + Labs)** • Aspect ratio, utilization factor, power planning **(Theory + Labs)** • Pre-placed cell tap cell, macro, memory/IP placement **(Theory + Labs)**	**Mr. Kunal P Ghosh** **(Director, VSD Corp. Pvt. Ltd.)**
Module 03 ***Placement, Clock tree synthesis***	**Interactive Lecture 3**	**Placement, Clock tree synthesis, Routing and SI (Lab – Yosys, Graywolf, Qrouter, OpenSTA, MAGIC)** • Placement STA with clock ideal (**Theory + Labs**) • CTS quality check – skew, pulse width, duty cycle, latency (**Theory + Labs**) • Routing quality check – signal integrity, delta delay, glitch (**Theory + Labs**) • DRC, LVS check and fix (**Theory + Labs**)	**Mr. Kunal P Ghosh** **(Director, VSD Corp. Pvt. Ltd.)**
Module 04 ***Global routing and Detailed routing***	**Interactive Lecture 4**	**Post-layout STA (Lab – OpenSTA)** • Types of setup/hold checks – reg2reg and IO, clock gating, recovery/removal, data-to-data, latch (time borrow/time given) **(Theory + Labs)** • Need of library, advanced ccs/ecsm concepts, variation (OCV, AOCV, SOCV in brief)	**Mr. Kunal P Ghosh** **(Director, VSD Corp. Pvt. Ltd.)**
	Interactive Lecture 5	**ECO (*Optional – Theory + Labs, Lab - TritonSizer*)** • Impact of ECO on power, performance and area • Margin based and slack based ECO for selective endpoints • PBA based ECO and leakage-recovery • Hierarchical and Physical aware ECO • Bottleneck analysis	**Mr. Kunal P Ghosh** **(Director, VSD Corp. Pvt. Ltd.)**
Module 05 ***Analog and Mixed Signal Circuit, Specifications to Design, Layout & GDS***	**Invited Talk 2**	**Important aspects, particular to Analog/Mixed signal IC design**. • Introduction and distinctions between discrete time and continuous time designs. • Example design with the basics of sampling, the effect of noise in sample and hold circuits. • Brief introduction and design of opamps, and multi-stage opamps. • Dealing with frequency compensations, noise and non-linearity in a multi-stage • opamp. Opamp offset cancellation techniques using mixed-signal methods like chopping and auto-zeroing.	**Dr. Imon Mondal** **(IIT Kanpur)**
	Invited Talk 3	• Switched Capacitor Circuits, Sample and Hold Circuits, Switched Capacitor Integrators, Switched Capacitor Differentiators, Switched Capacitor Filters • Layout Aspects of Switched Capacitor Circuits Floor Planning, Routing, DRC, DFM, ERC, LVS, Parasitic Extraction and GDSII	**Dr. Suhakumar Reddy** **(IIT Hyderabad)**
	Invited Talk 4	Issues and challenges in System on Chip Design, Digital design- back end flow/ physical design flow with Testing and packaging issues.	**Dr. H. S. Jatana** **(SCL Chandigarh)**
	Invited Talk 5	Design using SCL PDKS.	**Mr. Uday Khambate** **(SCL Chandigarh)**

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Detailed Schedule of the Programme

***Note: Inauguration on 08th July, 2019 at 9.00 am to 09:15am.**
Online Closing Ceremony on 12th July, 2019 from 05:45 pm onwards
***Break Timing:- Morning Tea Break : 11:00 am to 11:15 am**
Lunch Break: 01:15 pm to 02:00 pm
Evening Tea Break : 04:00 pm to 04:15 pm

***Note: 1) Interactive Lectures/ Invited Talk = 19 hrs**
2) Interactive Hands – on/Design-oriented/activity linked/Problem Solving/Case Studies sessions/ Quiz Test = 21 hrs

Date/Time	09:00 am to 11:00 am		11:15 am to 01:15 pm		02:00 pm to 04:00 pm		04:15 pm to 06:15 pm	
08-07-2019 Monday	**09:00 am to 09:30 am**	**09:30 am to 11:00 am**	**11:15 am to 12:15 pm**	**12:15 pm to 01:15 pm**	**02:00 pm to 03:00 pm**	**03:00 pm to 04:00 pm**	**Interactive Hands-on Session 1 (Continued)** To study the importance of standard cell library and design & characterize one cell using MAGIC Layout tool and ngSPICE for SPICE simulations.	
	Inauguration & Introduction with all remote centers	**Invited Talk 1 Dr. Anand Bulusu** (IIT Roorkee)	**Tool installation Session**	**Interactive Lecture 1 Mr. Kunal P Ghosh** (Director, VSD Corp. Pvt. Ltd.)	**Interactive Lecture 1** (Continued)	**Interactive Hands-on Session 1**		
09-07-2019 Tuesday	**Interactive Lecture 2 Mr. Kunal P Ghosh** (Director, VSD Corp. Pvt. Ltd.)		**Interactive Hands-on Session 2** To study various components of RISC-V microprocessor based SoC and review all components using MAGIC Layout tool.		**Interactive Hands-on Session 2 (Continued)**		**04:15 pm to 04:45 pm**	**04:45 pm to 06:15 pm**
							Quiz 01 (Based on Module 1 & 2)	**Interactive Lecture 3 Mr. Kunal P Ghosh** (Director, VSD Corp. Pvt. Ltd.)
10-07-2019 Wednesday	**Interactive Hands-on Session** 3 To do pre-layout timing analysis of SoC using OpenSTA, chip planning using MAGIC and block-level placement/routing using qflow RTL2GDS opensource EDA toolchain		**Interactive Hands-on Session 3 (Continued)**.		**Interactive Lecture 4 Mr. Kunal P Ghosh** (Director, VSD Corp. Pvt. Ltd.)		**Interactive Hands-on Session 4** To do hierarchical placement/routing using pads and blocks, and perform sign-off checks viz. LVS/DRC using Magic	
11-07-2019 Thursday	**Invited Talk 2 Dr. Imon Mondal** (IIT Kanpur)		**Invited Talk 4 Dr. H. S. Jatana** (SCL Chandigarh)		**02:00 pm to 03:00 pm**	**03:00 pm to 04:00 pm**	**Interactive Lecture 5 Mr. Kunal P Ghosh** (Director, VSD Corp. Pvt. Ltd.)	
					Invited Talk 4 (Continued)	**Interactive Hands-on Session 4 (Continued)**		
12-07-2019 Friday	**09:00 am to 10:00 am**	**10:00 am to 11:00 am**	**Interactive Hands-on Session 5** To perform post-layout timing analysis using OpenSTA and engineering change order (ECO) using Tritonsizer.		**Interactive Hands-on Session 5 (Continued)** To perform post-layout timing analysis using OpenSTA and engineering change order (ECO) using Tritonsizer.		**04:15 pm to 05:15 pm**	**05:15 pm to 05:45 pm**
	Invited Talk 3 Dr. Suhakumar Reddy (VEDA IIT Hyderabad)	**Interactive Lecture 5 (Continued) Mr. Kunal P Ghosh** (Director, VSD Corp. Pvt. Ltd.)					**Invited Talk 5 Mr. Uday Khambate** (SCL Chandigarh)	Quiz 02 (Based on Module 3, 4 & 5) and Lab Evaluation/ Manual Submission

List of Practical's for "VLSI Chip Design Hands on using open source EDA" Course

Sr. No.	List of Interactive Hands-on to "VLSI Chip Design Hands on using open source EDA"	Sessions
1)	**Aim:** To study the importance of standard cell library and design & characterize one cell using MAGIC Layout tool and ngSPICE for SPICE simulations. • System-on-Chip (SoC) planning and design concepts overview • Physical design overview • Why Libraries are called the soul and heart of semi-conductor industry? • Standard cells library overview • Art of layout – Stick diagram + Euler's path using MAGIC • Characterization of important parameters using ngSPICE	Interactive Hands-on Session 01 (3 hours session)
2)	**Aim:** To study various components of RISC-V microprocessor based SoC and review all components using MAGIC Layout tool. • Brief introduction RISC-V ISA • Overview of RISC-V based micro-processor and its related SoC • Overview of QFN48 package, pads, macros and memory in MAGIC • Idea of chip-planning, aspect ratio, utilization factor, power planning, decoupling capacitor, pads/memory and macro placement • Pros and cons of good-bad floorplan • Introduction to lab to create floorplan for small design, which will be covered in detail on Day 4)	Interactive Hands-on Session 02 (4 hours session)
3)	**Aim:** To do pre-layout timing analysis of SoC using OpenSTA, chip planning using MAGIC and block-level placement/routing using qflow RTL2GDS opensource EDA toolchain. • Logic synthesis and high fanout net synthesis interactive tutorial using Yosys opensource synthesis tool • Introduction to static timing analysis and the related Industry standard reporting formats • Pre-layout timing analysis of a design using OpenSTA opensource STA tool, which includes setup timing analysis for reg2reg and IO • Introduction to clock tree synthesis (CTS) and its related checks viz. skew, latency, pulse-width, duty cycle • Placement/Routing/CTS of a design using qflow opensource RTL2GDS tool • Perform CTS quality and routing quality checks using OpenSTA	Interactive Hands-on Session 03 (4 hours session)
4)	**Aim:** To do hierarchical placement/routing using pads and blocks, and perform sign-off checks viz. LVS/DRC using Magic • Full chip integration using MAGIC for a design with blocks and pads. • Revise floorplan from Day 2 • Populate layout from library manager in MAGIC, select digital core block and additional pads • Arrange pads and create a pad-frame hierarchy • Abut pads to ensure Padframe is DRC clean • Start manual Signal routing and power routing, tie-down unused inputs	Interactive Hands-on Session 04 (3 hours session)

	• Add substrate contacts, antenna diodes and pin—labels • Review completed layout and perform LVS/DRC checks	
5)	**Aim:** To perform post-layout timing analysis using OpenSTA and engineering change order (ECO) using Tritonsizer. • Introduction to clock generation and clock arrival time definitions • Introduction to IO constraints for interface analysis • Introduction to clock slew and data slew constraints • Code all above in SDC (Synopsys Design Constraints) format • Compute slack, CPPR (pessimism) and review its impact in OpenSTA • Interface and clock gating analysis • Asynchronous data checks and latch timing analysis • Impact of ECO on power, performance and area	Interactive Hands-on Session 05 (4 hours session)

Note: 1) Labs will follow the theory.

2) List of open-source EDA tools used for labs.

Tools installed:	
vsdflow	https://github.com/kunalg123/vsdflow.git
RePlaCe	https://github.com/abk-openroad/RePlAce.git
TritonSizer	https://github.com/abk-openroad/TritonSizer.git

1. 'vsdflow' is the TCL engine which installs all necessary open-source EDA tools and its respective dependencies (on ubuntu) needed for workshop. Steps to install are mentioned in the above link
2. List of tools covered in 'vsdfow'
    1. Yosys – for Synthesis
    2. Graywolf – for Placement
    3. Qrouter – for Routing
    4. Netgen – for LVS
    5. Magic – for Layout and Floorplanning
    6. Qflow – RTL2GDS integration
    7. OpenSTA & Opentimer – Pre-layout and Post-layout Static timing analysis
3. There will be some additional PDK's and scripts needed for workshop, which will downloaded LIVE.
4. For additional help to install all tools on Windows using Linux virtual box, students can refer to below course

https://www.vlsisystemdesign.com/vsd-a-complete-guide-to-install-open-source-eda-tools/