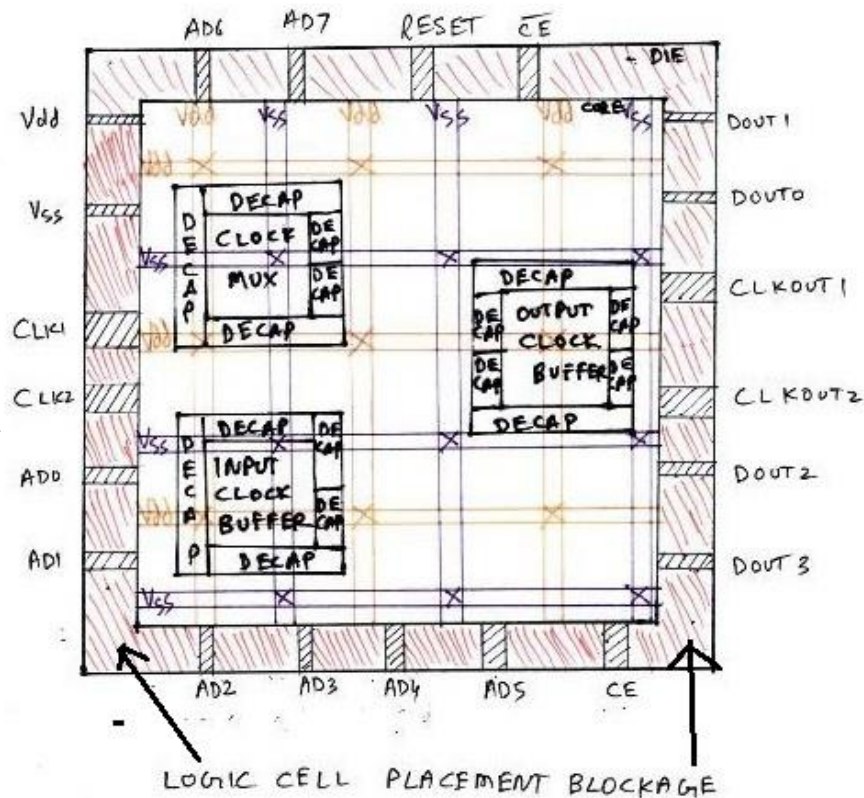




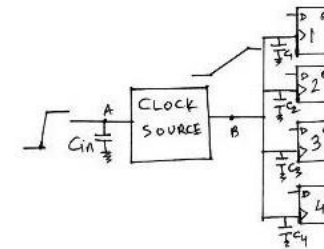
Open-source EDA community building using technology-mediated learning

Kunal Ghosh & Anagha Ghosh
VLSI System Design

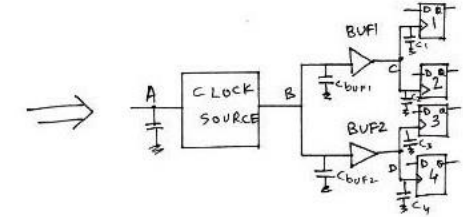




ASSUME $C_1 = C_2 = C_3 = C_4 = C_{BUF1} = C_{BUF2} = 1F$

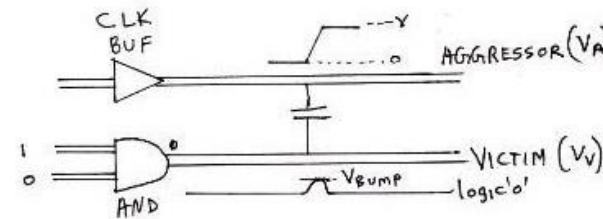


Total Capacitance at B \Rightarrow
 $C_{TOTB} = C_1 + C_2 + C_3 + C_4$
 $= 1 + 1 + 1 + 1$
 $= 4F$



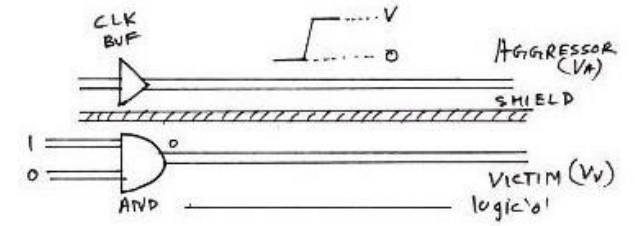
Total Capacitance at B
 $C_{TOTB} = C_{BUF1} + C_{BUF2}$
 $= 1 + 1 = 2F$
 Total Capacitance at C
 $C_{TOTC} = C_1 + C_2$
 $= 1 + 1 = 2F$
 Total Capacitance at D
 $C_{TOTD} = C_3 + C_4$
 $= 1 + 1 = 2F$

CLOCK TREE SYNTHESIS



IF $V_{BUMP} > V_{THRESHOLD}$
 $V_V = \text{logic '1'} \Rightarrow \text{'V'}$

\Rightarrow FUNCTIONALITY CHANGE OF AND GATE



No BUMP
 $V_V = \text{logic '0'} \Rightarrow \text{'0'}$

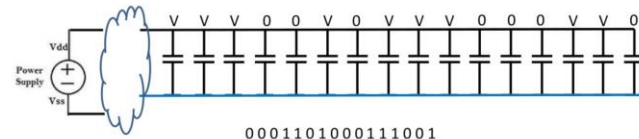
\Rightarrow NO FUNCTIONALITY CHANGE OF AND GATE

\Rightarrow COST \Rightarrow AREA INCREASE DUE TO ADDITION OF SHIELD



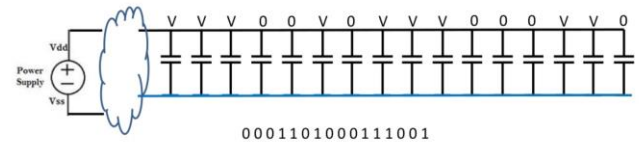
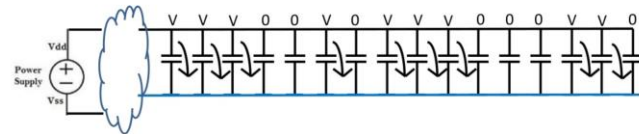
Can you see voltage droop and ground bounce? – Infographics

“An idea sketched to us by Srikanth Jadcherla”



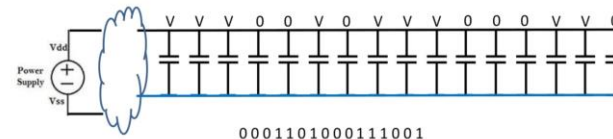
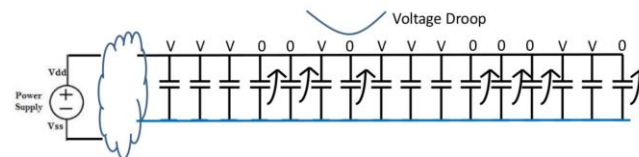
What does this mean?

This means, all capacitors which were charged to 'V' volts will have to discharge to '0' volts through single 'Ground' tap point. This will cause a bump in 'Ground' tap point.



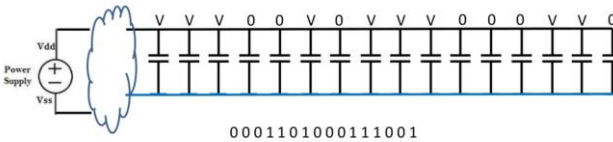
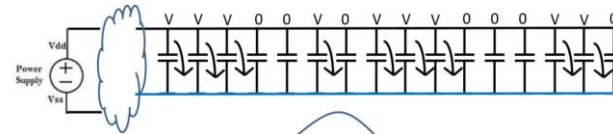
What does this mean?

Also, all capacitors which were '0' volts will have to charge to 'V' volts through single 'Vdd' tap point. This will cause lowering of voltage at 'Vdd' tap point.



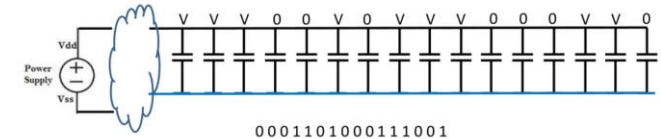
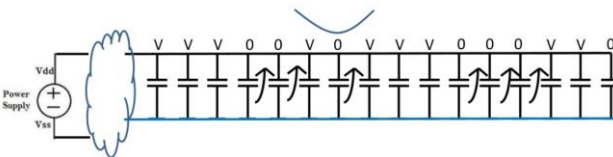
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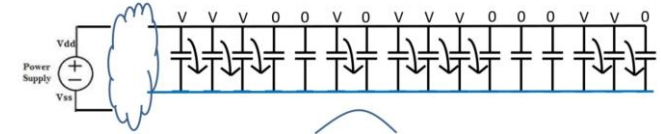
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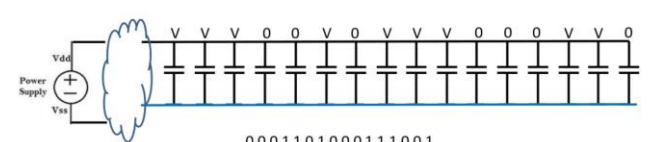


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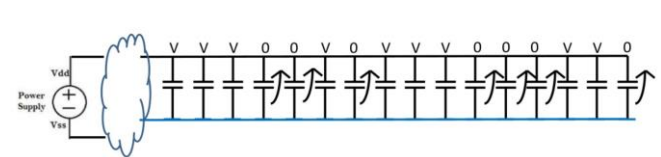


Ground Bounce

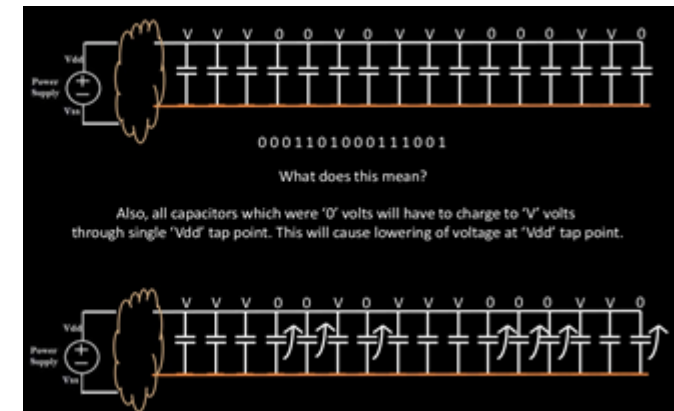
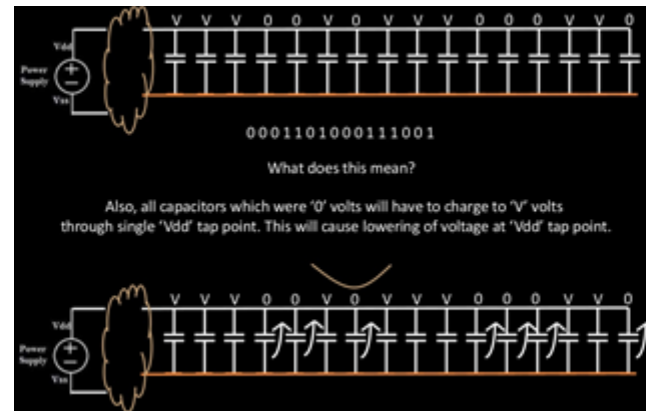
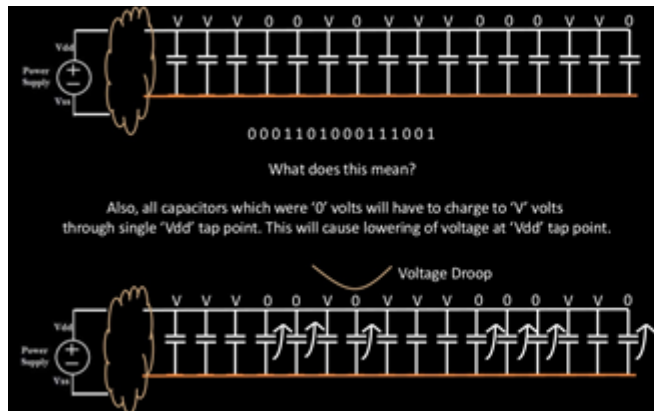
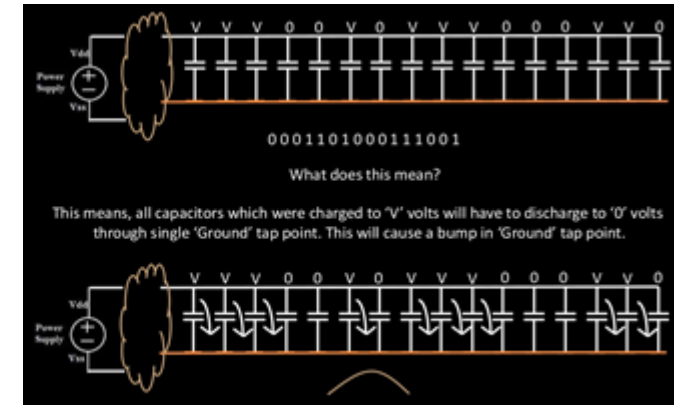
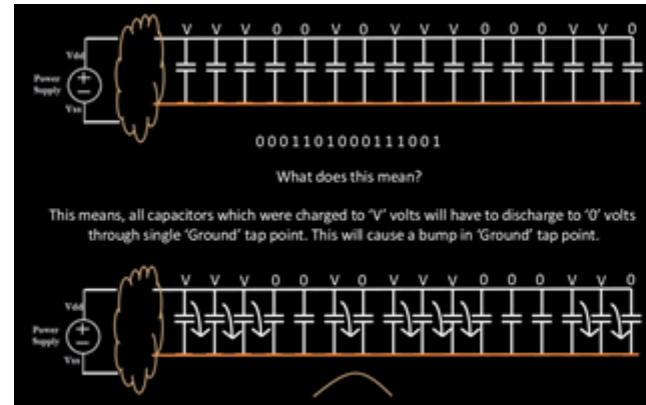
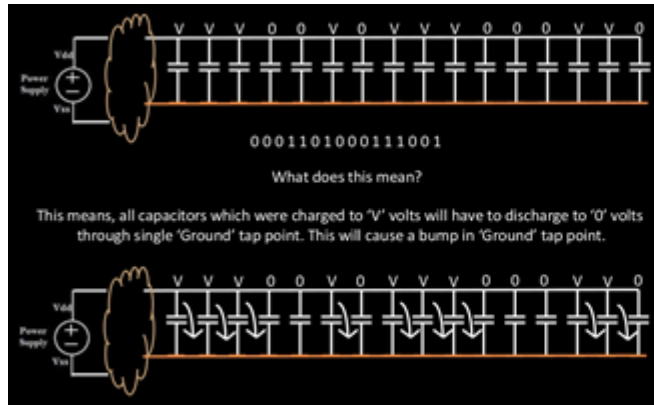


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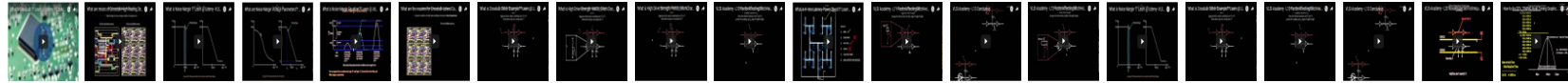


Black board looked brighter than white
“An idea seemed to be working with Khan Academy”

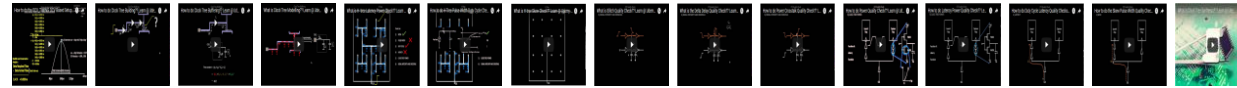


Launched 4 video courses, 2 FREE 2 PAID

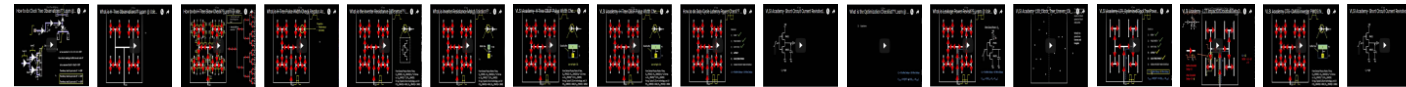
Signal integrity



VLSI Essential concepts and interview FAQ's



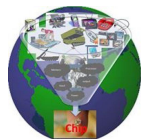
Clock tree synthesis – Part 1 & 2



Physical design flow



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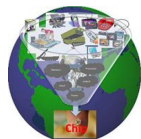


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Birth of Announcements

Promotional Announcements

Educational Announcements

Flipped classroom for VLSI & Semiconductors

"That's what we are being called by a Professor at IIT Bombay – Its really an honor"

Hi

I noticed you are looking for some real good alternative for classrooms where you can study and do labs while at home. So this mail might just be a useful one.

There are basically 3 primary reasons, you might just love the courses I built online –

You can study at your own pace. No hurry and no grading

You can put your queries forward in front of me as private message or in front of 13000 people who are already taking our courses. One of us will definitely get back to you in a day's time

You can download opensource EDA tools on your laptop, install them and learn from scratch. I have a course which explains how to download and install opensource EDA tools on your windows machine using Linux virtual box

Another really important reason why you might just choose the below courses on top of others, is its pricing. Month end is nearing, and I would like to offer up to 90% discount on all my courses. You might want to check out the links below **before it expires in next 18hours**

TCL Scripting –

https://www.udemy.com/vsd-tcl-programming-from-novice-to-expert/?couponCode=FLIPPED_CLASSROOM

STA Webinar –

https://www.udemy.com/vsd-static-timing-analysis-sta-webinar/?couponCode=FLIPPED_CLASSROOM

Library Characterization and modelling : Part 1 –

https://www.udemy.com/vlsi-academy-library-characterization-part-1/?couponCode=FLIPPED_CLASSROOM

2 promotional announcements per month



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graph TD
    A[Birth of Announcements] --> B[Promotional Announcements]
    A --> C[Educational Announcements]
    C --> D[Informational Announcements]
    C --> E[Instructional Announcements]
  
```


Educational Announcements

Talking about leakage power or static power, one classic definition that comes into our minds is that of sub-threshold leakage current, which can be replicated or explained through below image

The explanation of tunneling current needs a knowledge on energy band diagrams of a MOS capacitor system as shown below:

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The Udemy logo, featuring a large blue stylized 'U' with the word 'UDEMY' in black capital letters on a yellow rectangular background.

Power Characterization

Static Power (Leakage Power)

Tunneling current

The diagram illustrates the physical structure and energy band diagram of a MOSFET, focusing on the mechanism of tunneling current.

Physical Structure (Left): A cross-sectional view of a MOSFET. It shows a **P-substrate** with two **n⁺** regions (source and drain). A **Gate oxide** layer is grown over the channel, and a **Poly-Si or metal gate** is deposited on top. The gate is connected to a terminal labeled **G**.

Energy Band Diagram (Right): A vertical energy band diagram showing the energy levels across the device. The **Free electron level** is indicated at the top. The **SiO₂** layer is shown on the left, and the **P-type Silicon** is on the right. The **Metal** gate is shown in the center. The energy levels are labeled: **Ec** (Conduction band edge), **E_f** (Fermi level), and **Ev** (Valence band edge). The **Gate oxide thickness (Tox)** is indicated by a red arrow. The **Bandgap (Ec - Ev)** is indicated by a yellow arrow. The **Barrier height (Ec - Ef)** is indicated by a red arrow. The **Band bending** is shown by the sloping lines. The **Electron tunneling** is indicated by a red arrow pointing from the **E_f** level into the **Ec** level through the **SiO₂** barrier.

So, in a MOS system, the metal gate and P-type silicon has fermi energy level, which are at different energy values. Now when 2 different systems with 2 different fermi levels are connected across SiO₂, at thermal equilibrium when there are no currents flowing, the fermi-level of all the components attached are expected to be at same level, and while that process, the energy band of P-type silicon at the Oxide-

A funnel diagram with a globe at the top. Inside the funnel, there are various icons representing different aspects of China, such as a map, a person, a building, and a car. The funnel narrows down to a red box at the bottom with the word 'China' in white.

Only course enrollment was not enough – course completion needed
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Ashok Kalbag

Lab work and Blue chip
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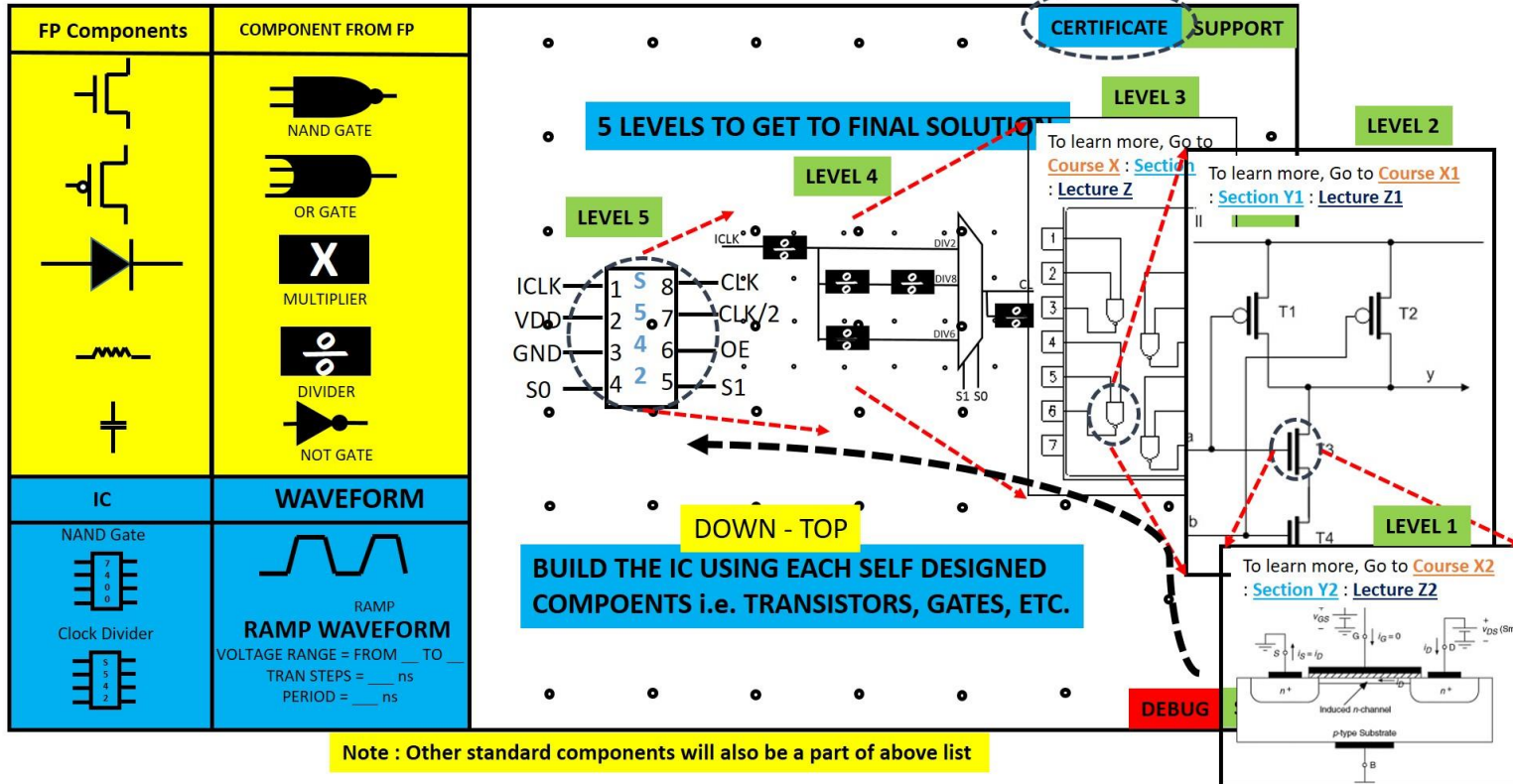
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*FP – FIRST PRINCIPLE



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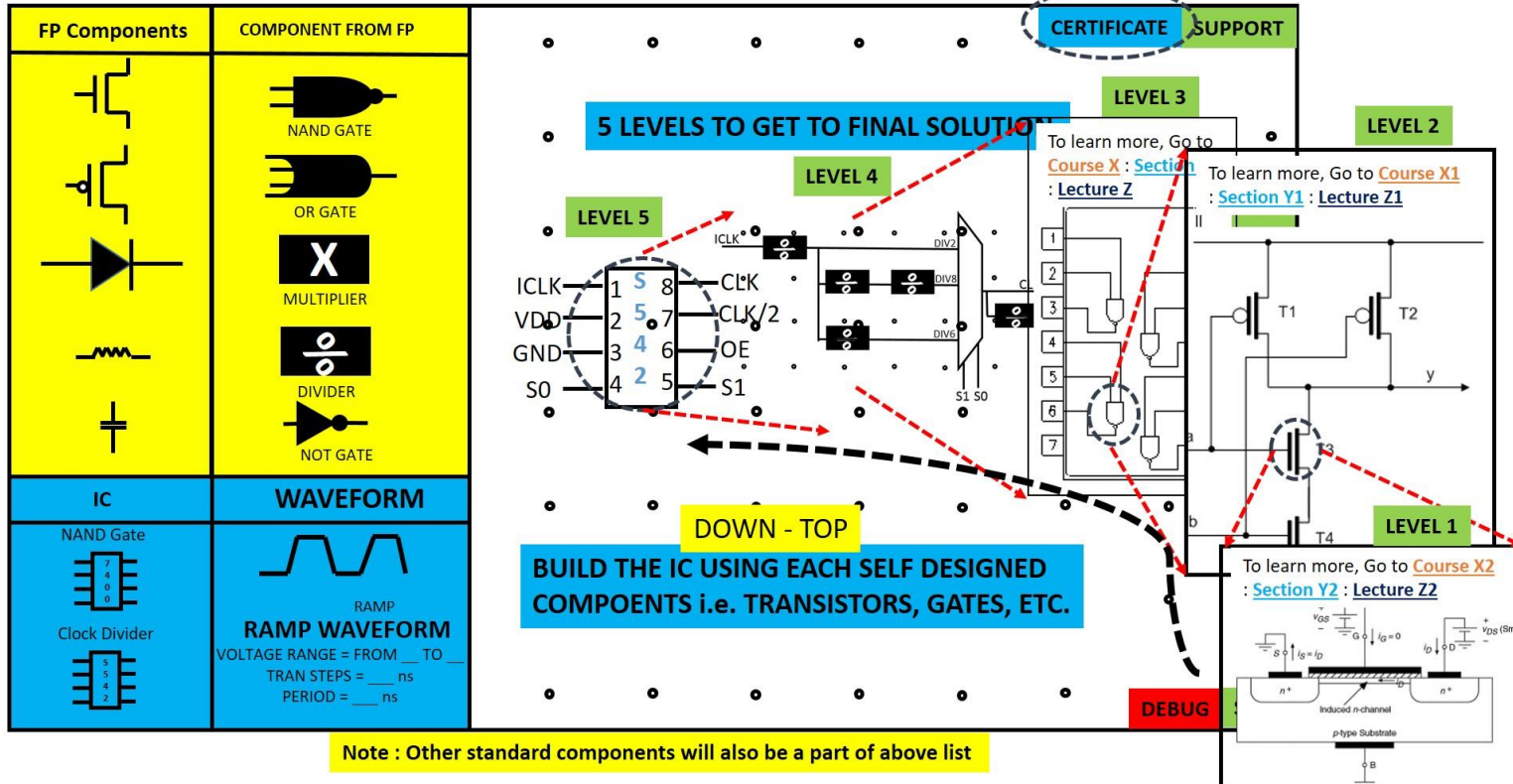
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Designed in 2015
Still work in progress
Waiting to finish relevant courses



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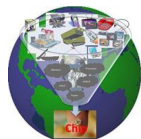
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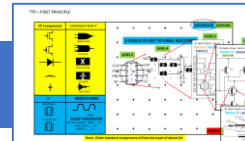
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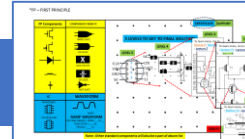


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“An idea chalked with Mohamed Kassem”

Mohamed Kassem

Guide for Blended learning concept
and open-source tool integration



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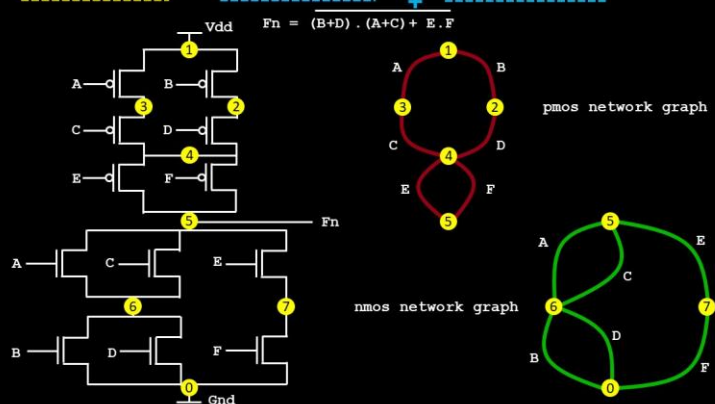
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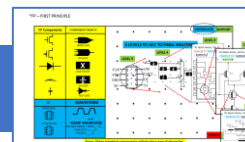


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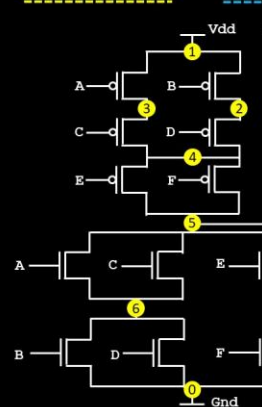
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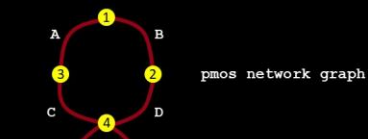
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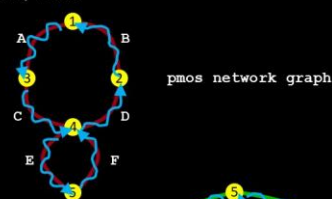
$$F_n = (B+D) \cdot (A+C) + E \cdot F$$



pmos network graph

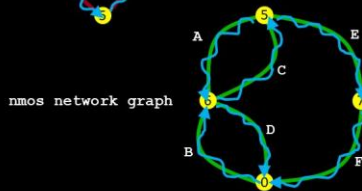
Art of layout - Euler's path and stick diagram

$$F_n = (B+D) \cdot (A+C) + E \cdot F$$

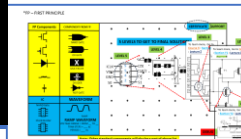


pmos network graph

A - C - E - F - D - B



nmos network graph



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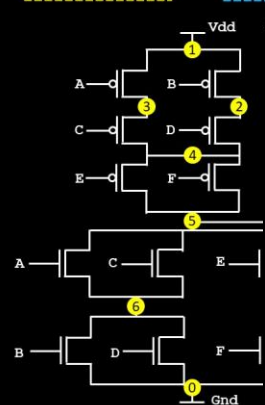
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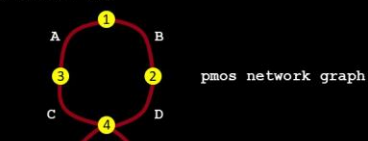
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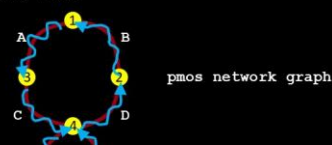


$$F_n = (B+D) \cdot (A+C) + E \cdot F$$



Art of layout - Euler's path and stick diagram

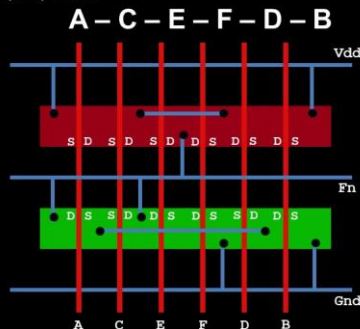
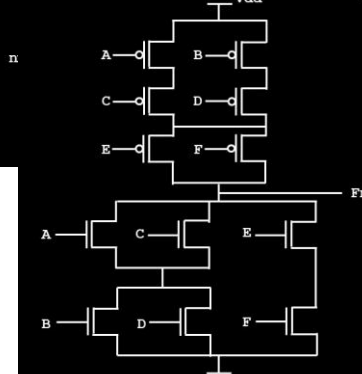
$$F_n = (B+D) \cdot (A+C) + E \cdot F$$



A - C - E - F - D - B

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$$F_n = (B+D) \cdot (A+C) + E \cdot F$$



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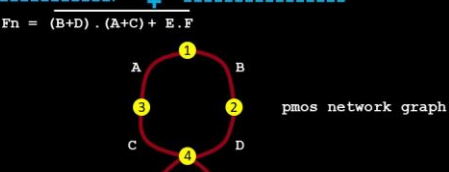
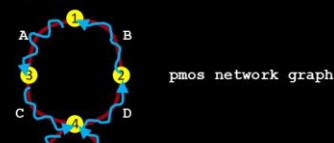


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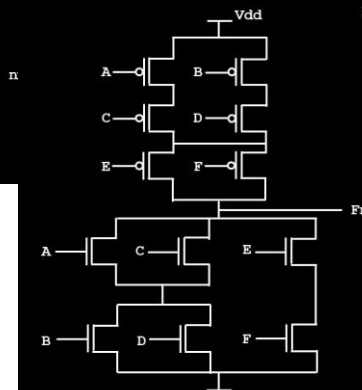
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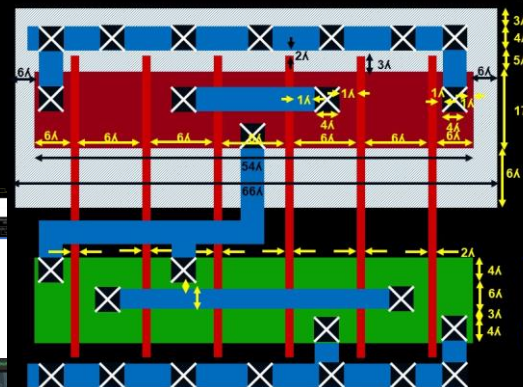
The diagram illustrates a 6T1S SRAM cell. The top section shows the access transistors (A, C, E) and storage transistors (B, D, F) connected to Vdd and Gnd. The bottom section shows the cross-coupled inverters (A-C and B-D) with nodes C and D. Nodes are numbered 1 to 9.


$$F_n = (B+D) \cdot (A+C) + E \cdot F$$


A-C-E-F-D-B

$$F_n = (B+D) \cdot (A+C) + E \cdot F$$


+ A-C-E-F-D-B



details (min)	Design rule
poly width	2λ
extension over active	3λ
poly to active spacing	1λ
poly to ndc spacing	1λ
ndc width	4λ
metal width	3λ
poly to metal spacing	n/a
ndc to ndc spacing	2λ
active/diffusion width	3λ

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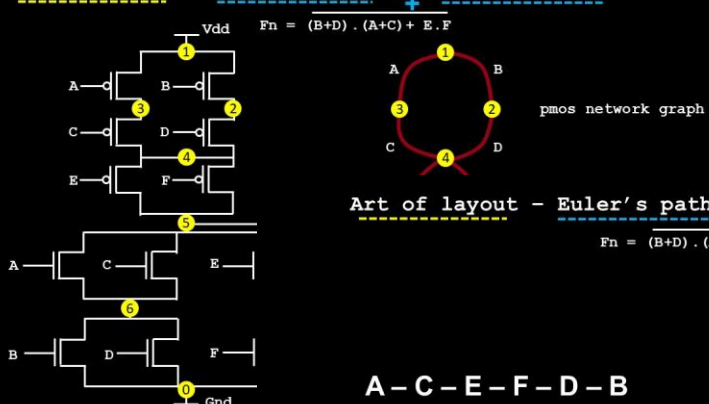
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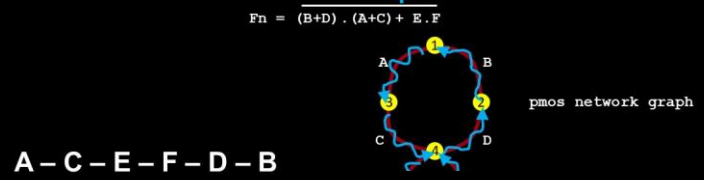
Year - 2011



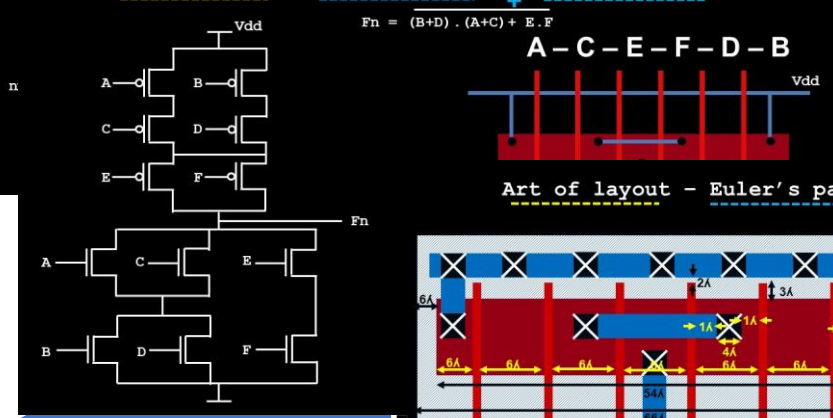
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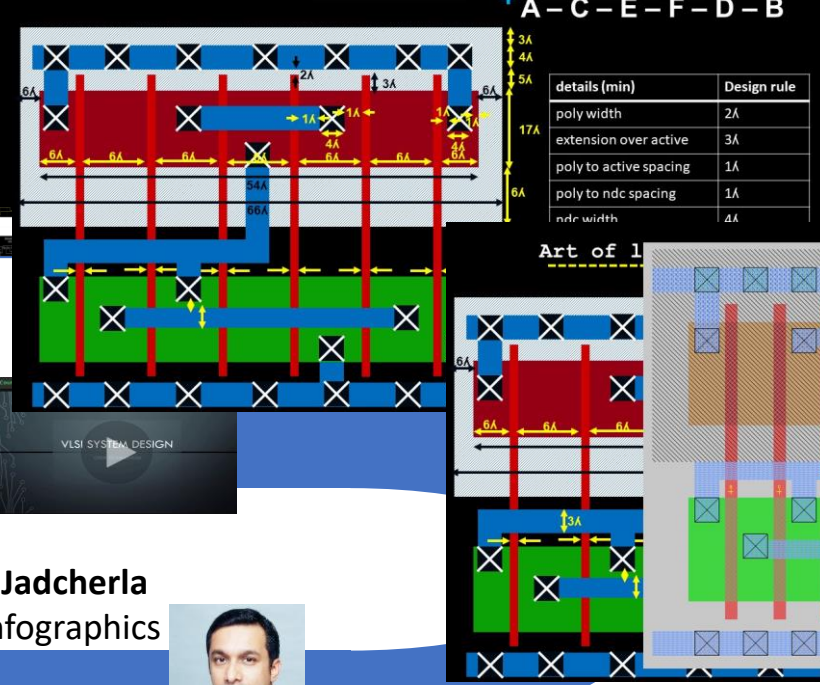
Art of layout - Euler's path and stick diagram



Art of layout - Euler's path and stick diagram

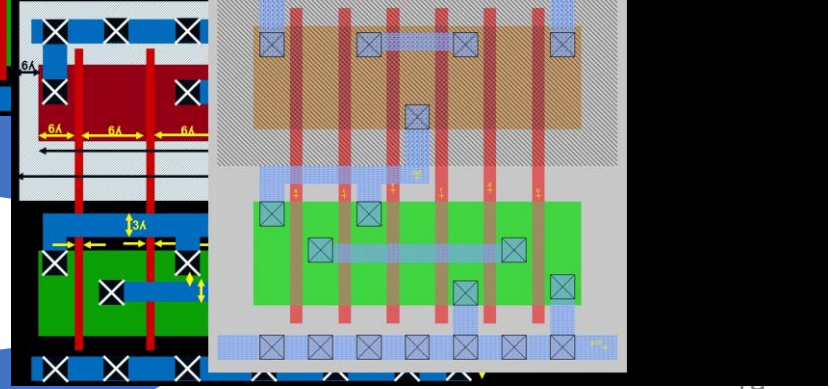


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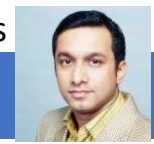
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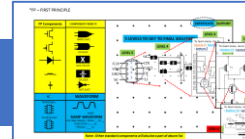
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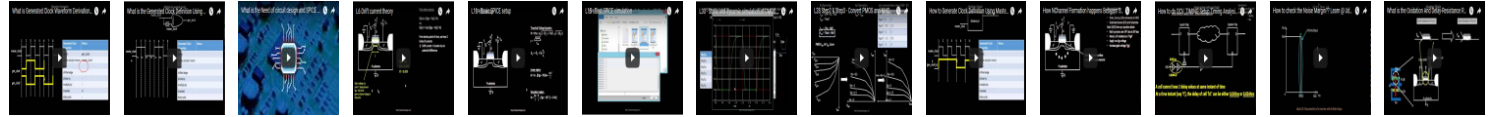
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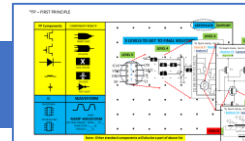
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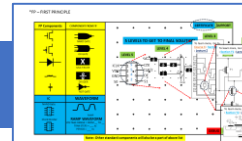
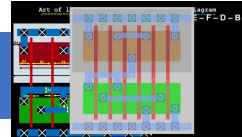
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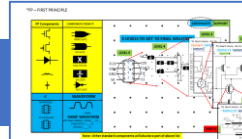
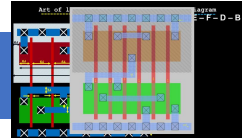


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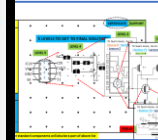
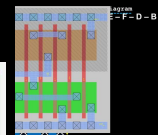
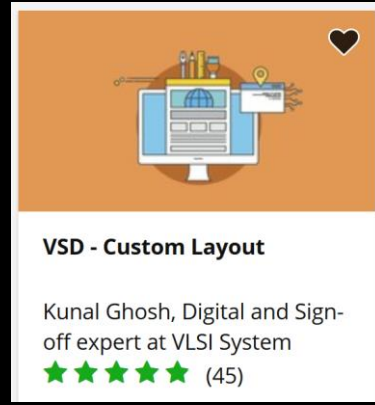


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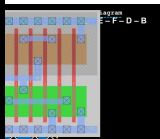
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VSD - Custom Layout

Kunal Ghosh, Digital Design expert at VLSI



VSDFLOW. As a prototype, currently VSDFLOW uses toolset shown in below figure no. 1

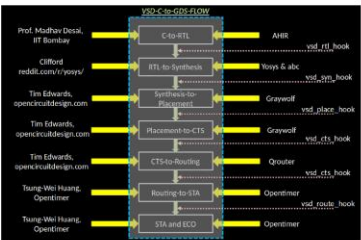


Figure 1: VSDFLOW framework

VSDFLOW is designed in such a flexible way, that user can pitch-in at any point of flow and some of them are enumerated below:

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Figure 2: Different constraints format

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Results

We have tested VSDFLOW with OSU 180nm technology and below designs show the results in terms of performance and area

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This is a synthesizable 16bit microcontroller core which is written in Verilog and available at opencores.org

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Table 1: openMSP430 (by opencores.org)

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An example system of MCU which contains a single cortex-m0

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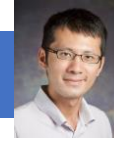
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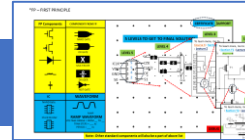
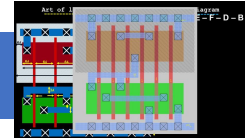
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Types of setup/hold analysis

1. reg2reg
2. in2reg
3. reg2out
4. in2out
5. clock gating
6. recovery/removal



VSD - Static Timing Analysis - II

Kunal Ghosh, Digital and Sign-off expert at VLSI System

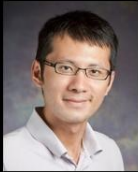
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Homework-

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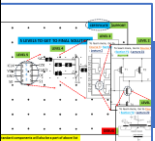
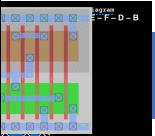




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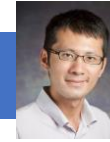
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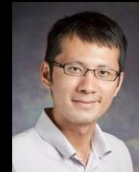
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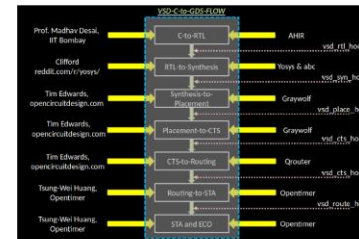


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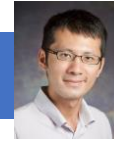
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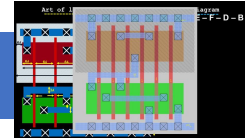
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United States	28%
Egypt	2%
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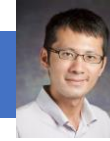


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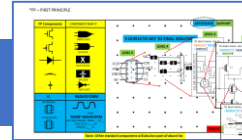
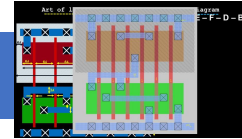
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