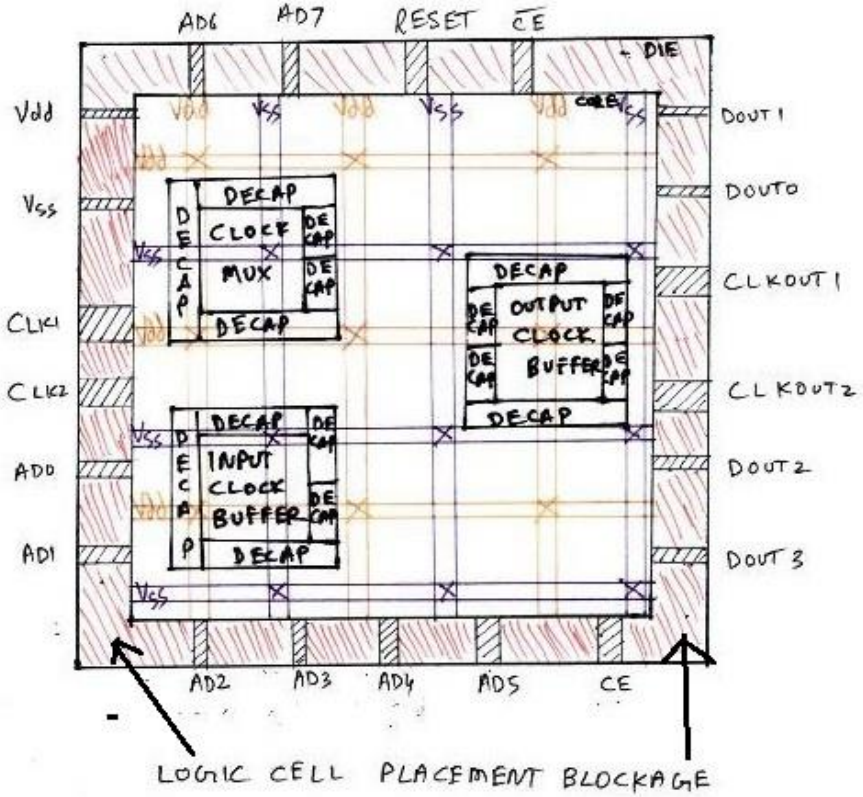
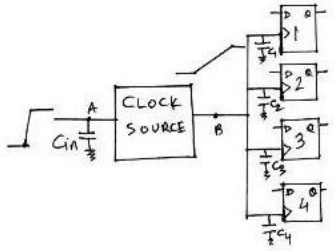
# Open-source EDA community building using technology-mediated learning

Kunal Ghosh & Anagha Ghosh
VLSI System Design




ASSUME $C_1 = C_2 = C_3 = C_4 = C_{BUF1} = C_{BUF2} = 1F$

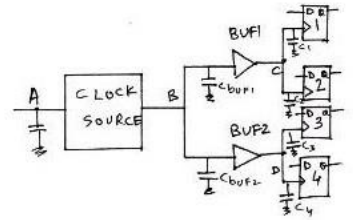



Total Capacitance at B ⇒

$C_{TOT_B} = C_1 + C_2 + C_3 + C_4$

$= 1 + 1 + 1 + 1$

$= 4F$




Total Capacitance at B

$C_{TOT_B} = C_{BUF1} + C_{BUF2}$

$= 1 + 1 = 2F$

Total Capacitance at C

$C_{TOT_C} = C_1 + C_2$

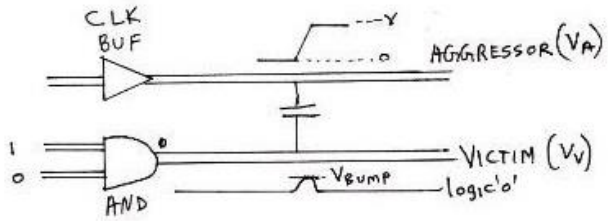
$= 1 + 1 = 2F$

Total Capacitance at D

$C_{TOT_D} = C_2 + C_4$

$= 1 + 1 = 2F$

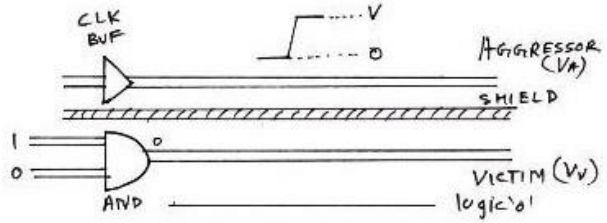
CLOCK TREE SYNTHESIS




IF $V_{Bump} > V_{THRESHOLD}$

$V_V$ = logic'1' ⇒ '1'v

⇒ FUNCTIONALITY CHANGE OF AND GATE




No Bump

$V_V$ = logic'0' ⇒ '0'v

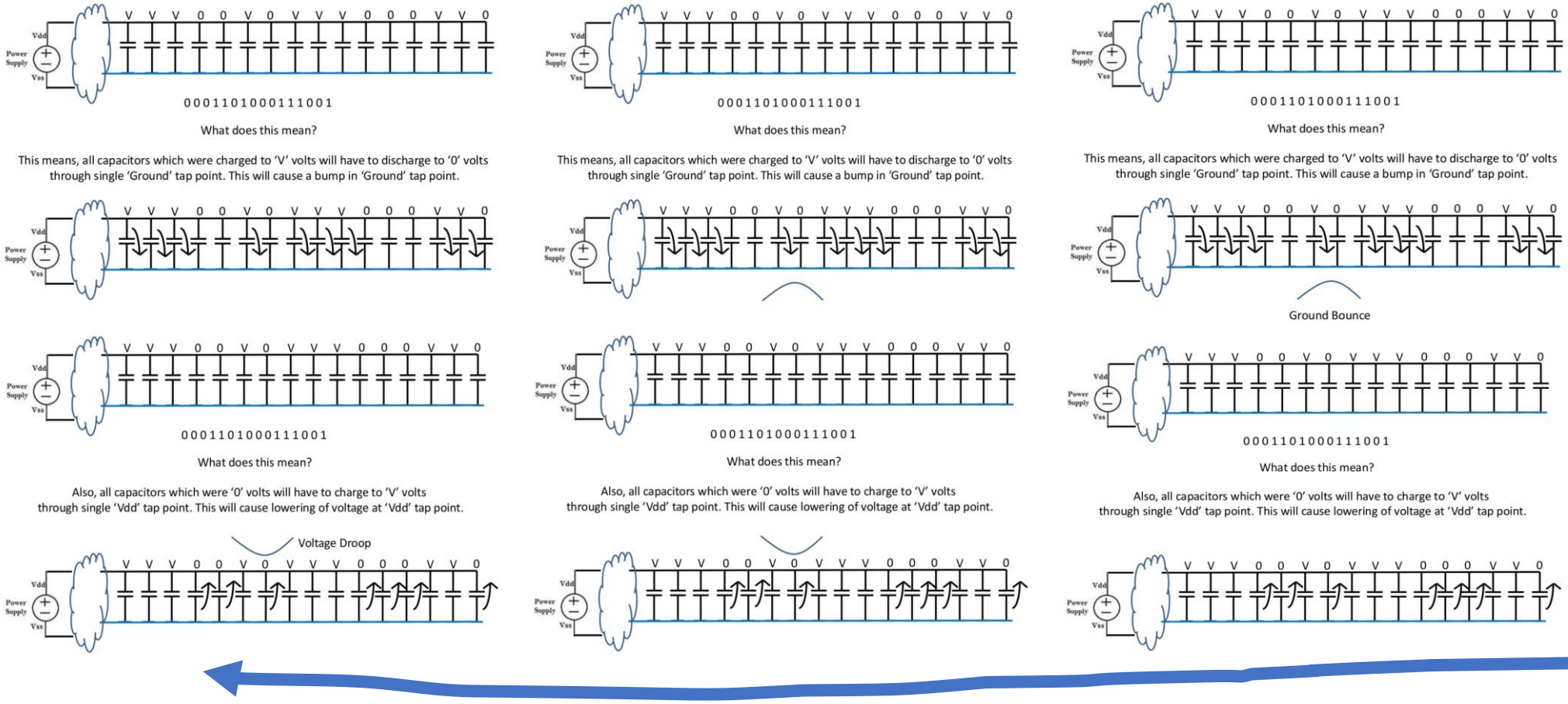
⇒ No FUNCTIONALITY CHANGE OF AND GATE

⇒ COST ⇒ AREA INCREASE DUE TO ADDITION OF SHIELD

CLOCK NET SHIELDING

# Can you see voltage droop and ground bounce? – Infographics

***"An idea sketched to us by Srikanth Jadcherla"***




**Srikanth Jadcherla**

Image2Infographics

https://www.vlsisystemdesign.com/

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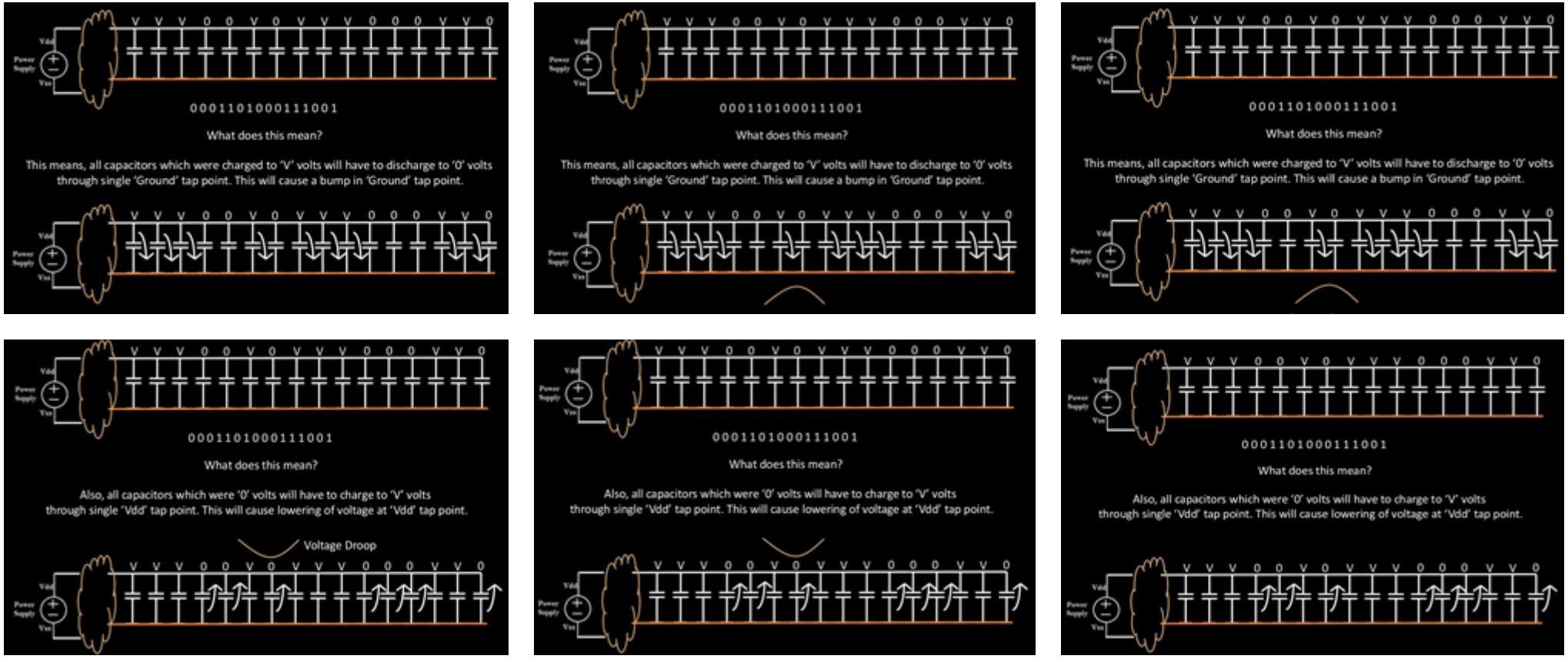
**Year - 2011**

Black board looked brighter than white

***"An idea seemed to be working with Khan Academy"***

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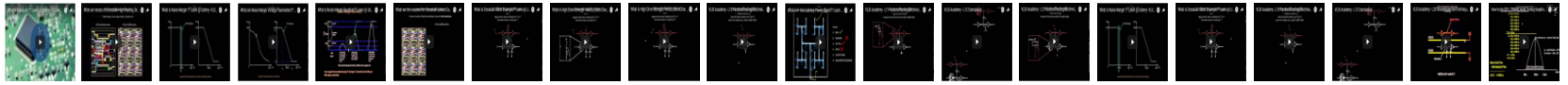
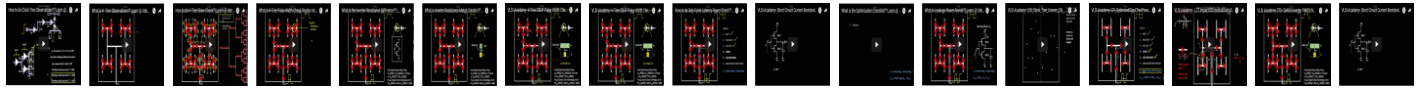
# Launched 4 video courses, 2 FREE 2 PAID

**Signal integrity**



**VLSI Essential concepts and interview FAQ's**

**Clock tree synthesis – Part 1 & 2**



**Physical design flow**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**Birth of Announcements**

**Promotional Announcements**

**Educational Announcements**

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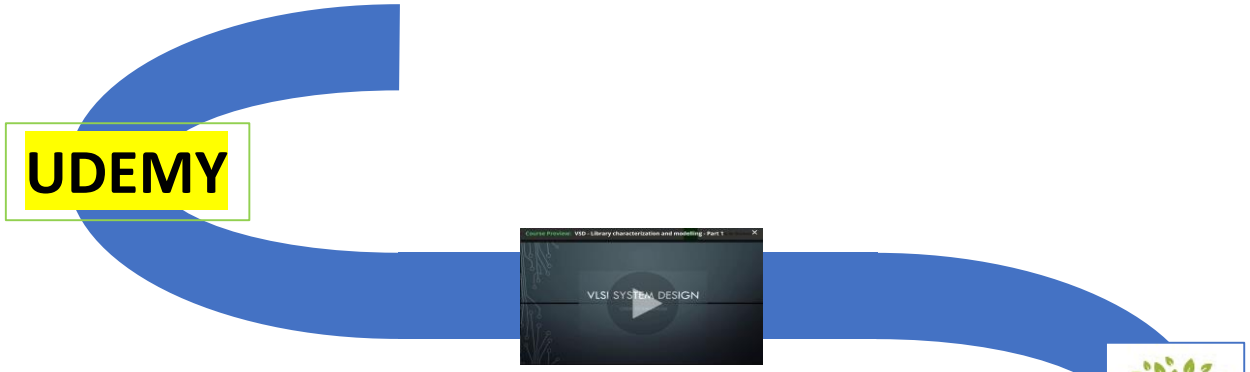
Newsletters, email marketing and course bundling

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## Birth of Announcements

**Promotional Announcements**

**Educational Announcements**

**Flipped classroom for VLSI & Semiconductors**

"That's what we are being called by a Professor at IIT Bombay – Its really an honor"

Hi

I noticed you are looking for some real good alternative for classrooms where you can study and do labs while at home. So this mail might just be a useful one.

There are basically 3 primary reasons, you might just love the courses I built online –

You can study at your own pace. No hurry and no grading

You can put your queries forward in front of me as private message or in front of 13000 people who are already taking our courses. One of us will definitely get back to you in a day's time

You can download opensource EDA tools on your laptop, install them and learn from scratch. I have a course which explains how to download and install opensource EDA tools on your windows machine using Linux virtual box

Another really important reason why you might just choose the below courses on top of others, is its pricing. Month end is nearing, and I would like to offer up to 90% discount on all my courses. You might want to check out the links below **before it expires in next 18hours**

**TCL Scripting –**

https://www.udemy.com/vsd-tcl-programming-from-novice-to-expert/?couponCode=FLIPPED_CLASSROOM

**STA Webinar –**

https://www.udemy.com/vsd-static-timing-analysis-sta-webinar/?couponCode=FLIPPED_CLASSROOM

**Library Characterization and modelling : Part 1 –**

https://www.udemy.com/vlsi-academy-library-characterization-part-1/?couponCode=FLIPPED_CLASSROOM

***2 promotional announcements*** **per month**

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**Year - 2011**

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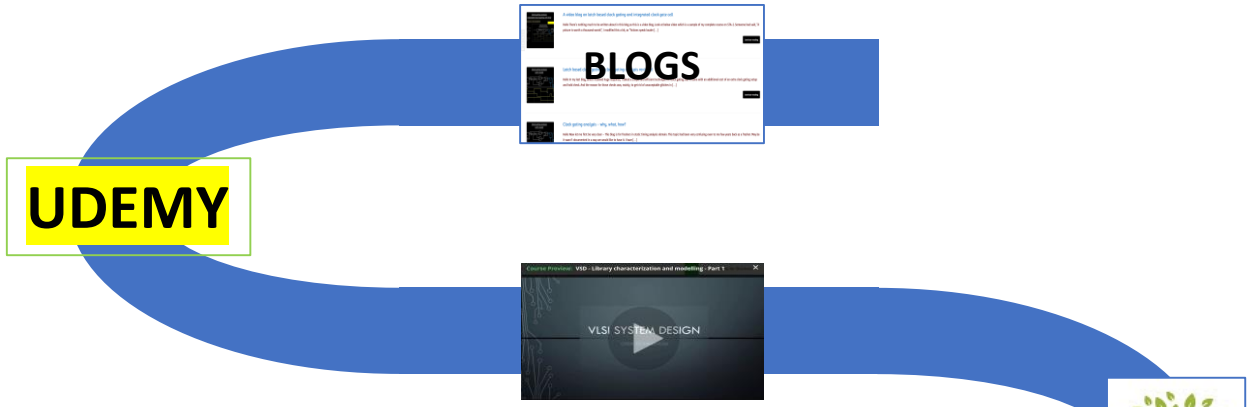


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## Birth of Announcements

**Promotional Announcements**

**Educational Announcements**

***4 educational announcements*** **per month**

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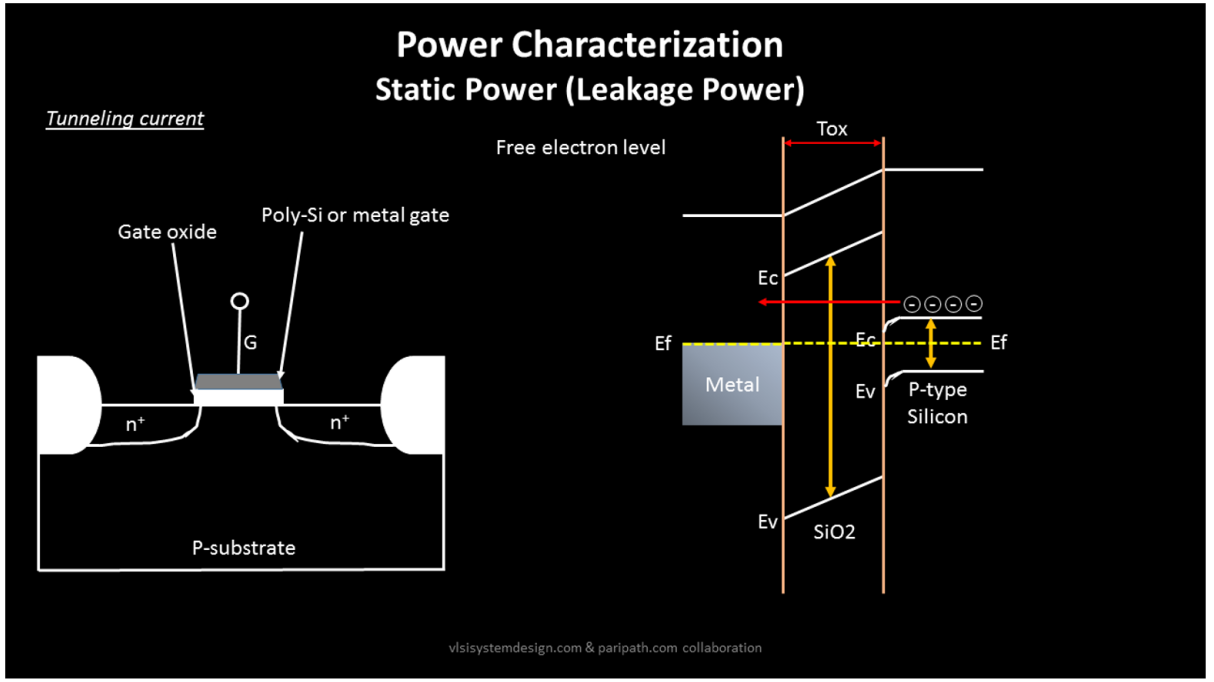
**Srika**
Imag

**Let's unveil few more static power**

Talking about leakage power or static power, one classic definition that comes into our minds is that of sub-threshold leakage current, which can be replicated or explained through below image

**Tunneling current:**

The explanation of tunneling current needs a knowledge on energy band diagrams of a MOS capacitor system as shown below:




So, in a MOS system, the metal gate and P-type silicon has fermi energy level, which are at different energy values. Now when 2 different systems with 2 different fermi levels are connected across SiO2, at thermal equilibrium when there are no currents flowing, the fermi-level of all the components attached are expected to be at same level, and while that process, the energy band of P-type silicon at the Oxide-

Only course enrollment was not enough – course completion needed

***"A seed planted in our heads by Ashok Kalbag – Labs and Design challenge"***

**Ashok Kalbag**
Lab work and Blue chip design challenge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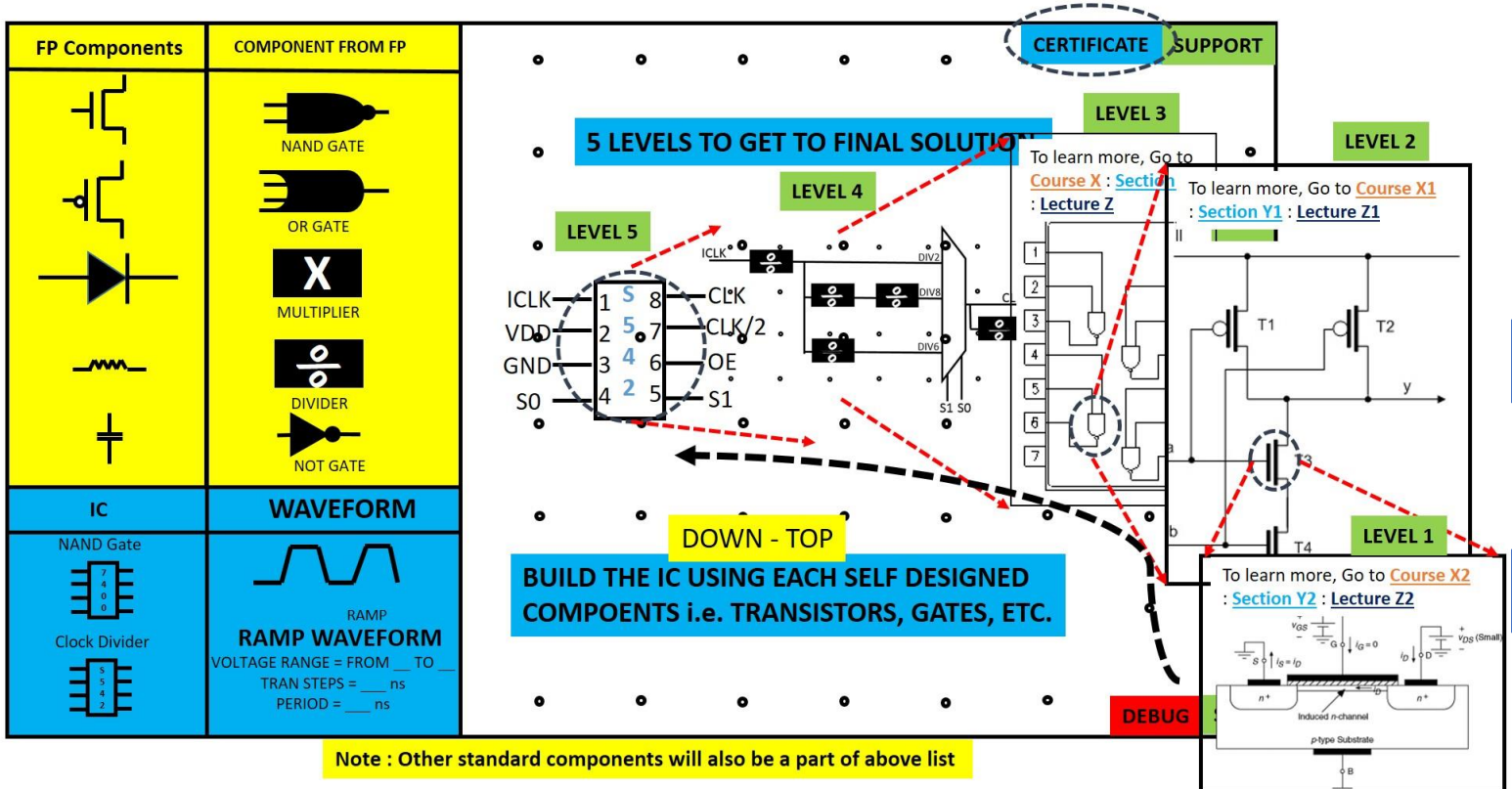
***"A seed planted in our heads by Ashok Kalbag – Labs and Design challenge"***

*FP – FIRST PRINCIPLE

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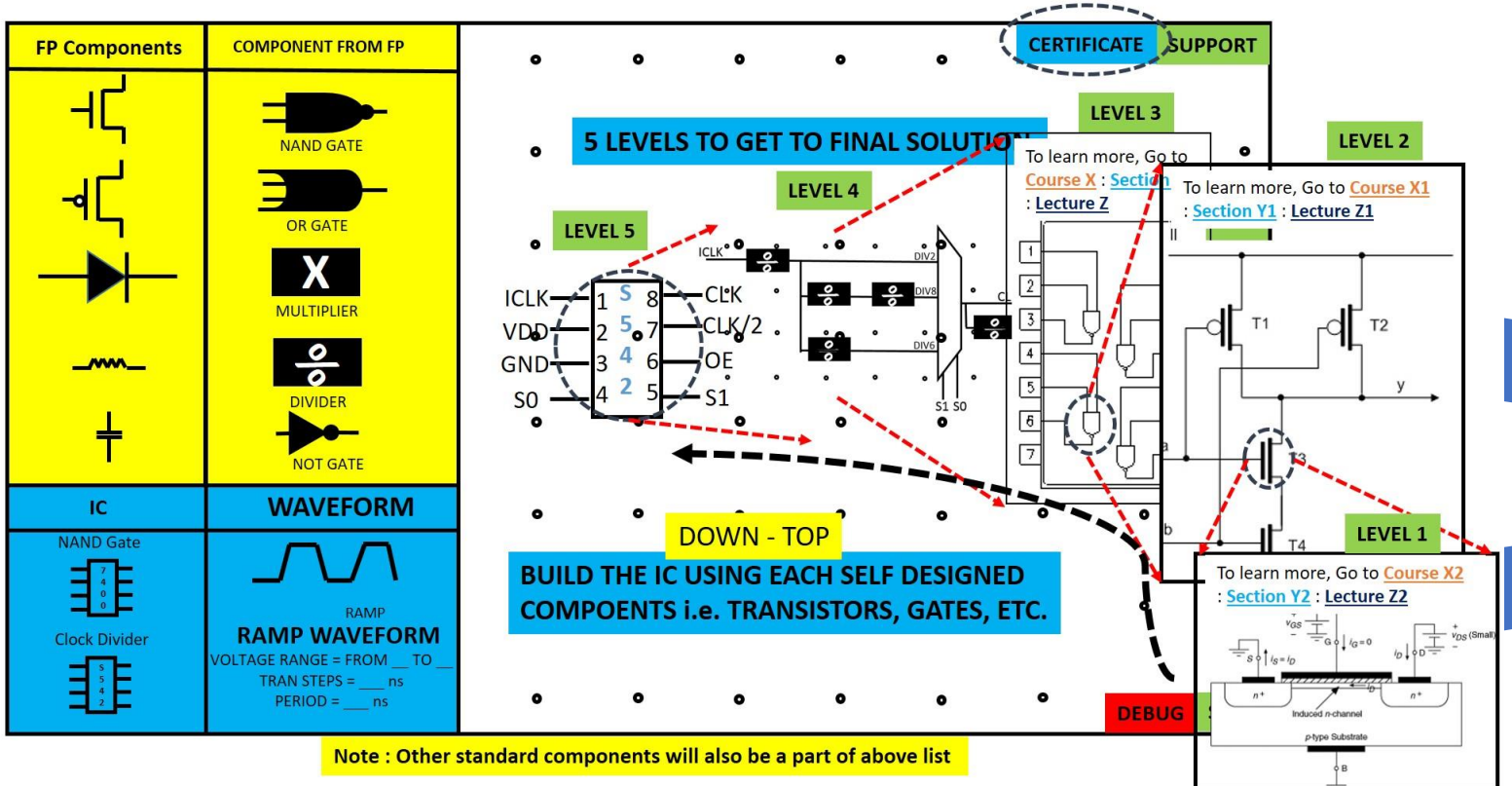


***Designed in 2015***
***Still work in progress***
***Waiting to finish relevant courses***

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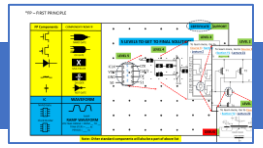

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***“An idea chalked with Mohamed Kassem”***

**Mohamed Kassem**
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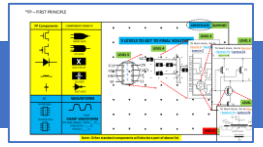

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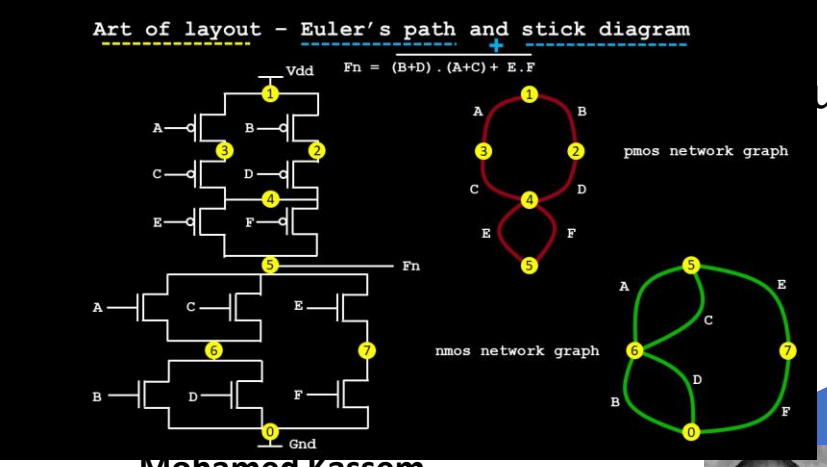


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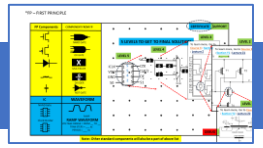

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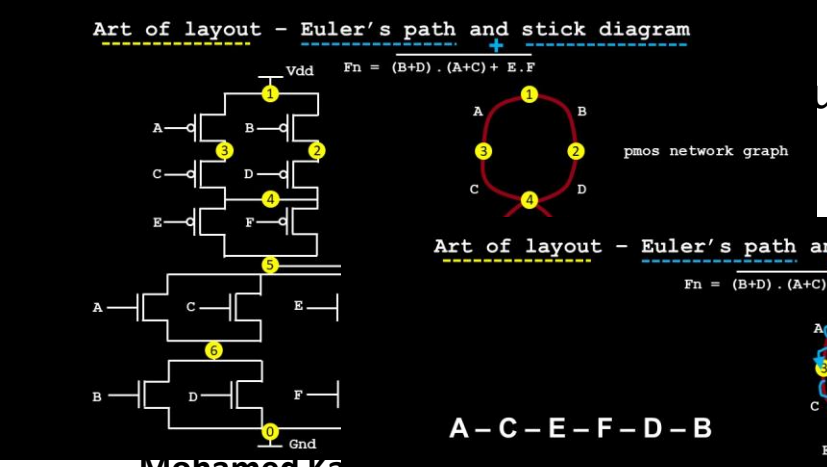


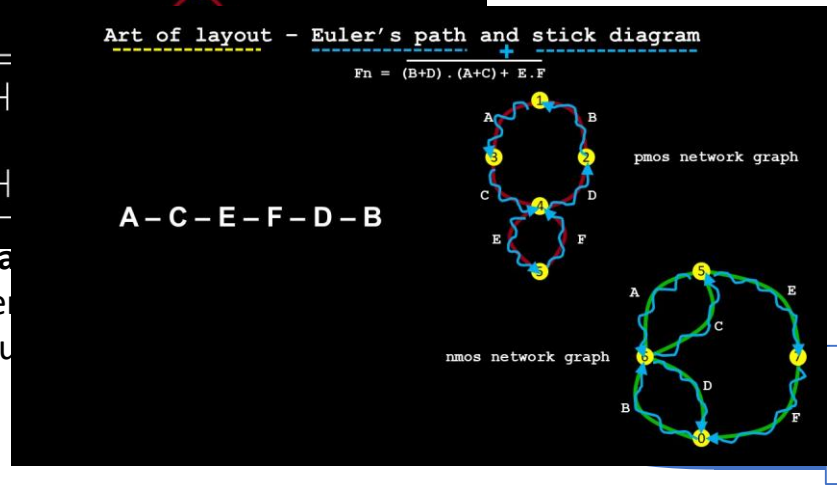


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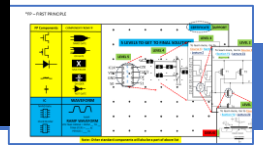

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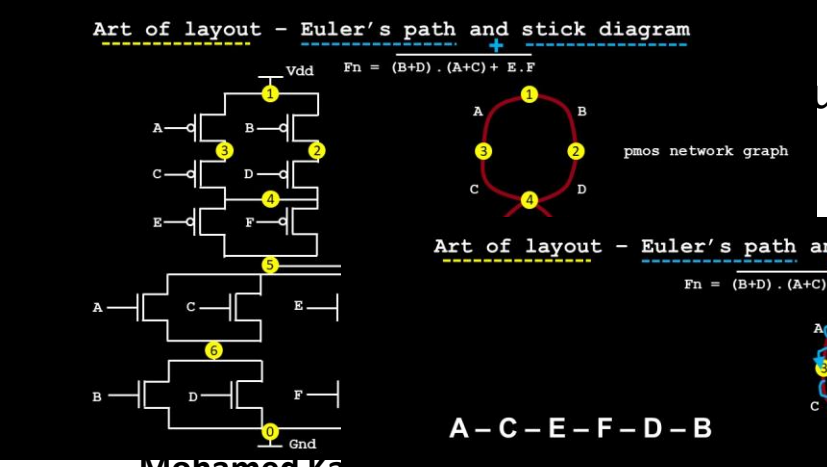


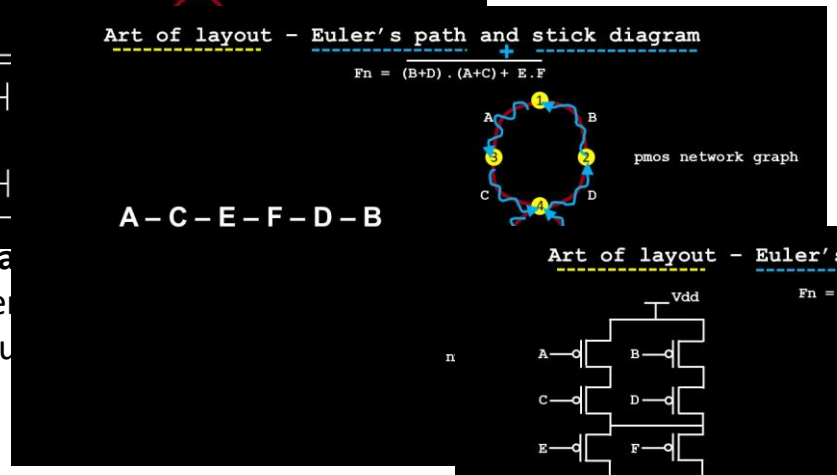


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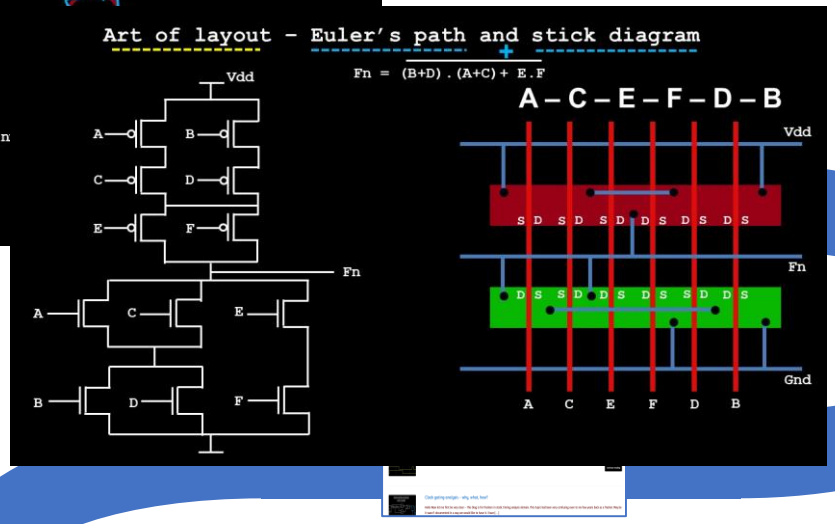


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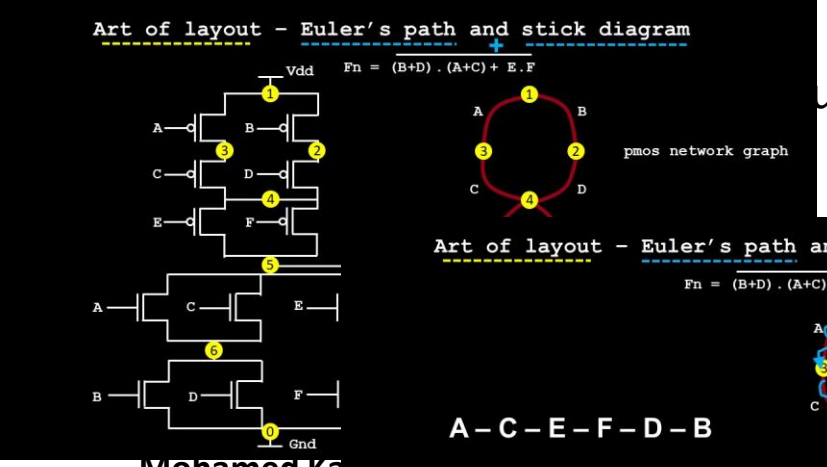


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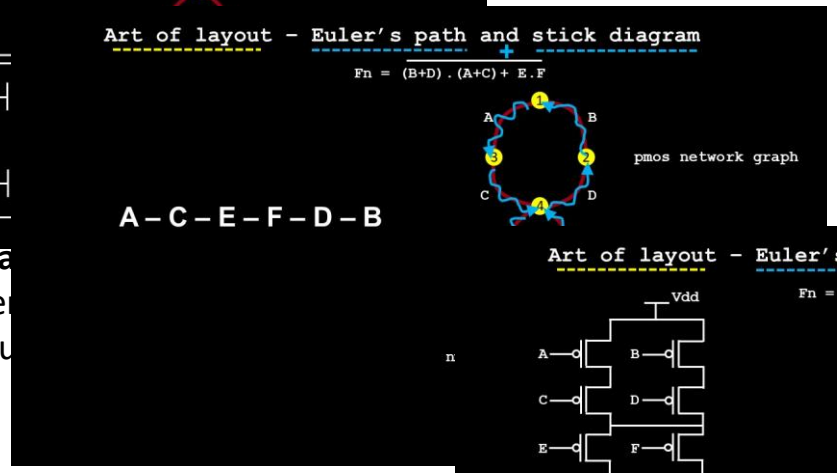


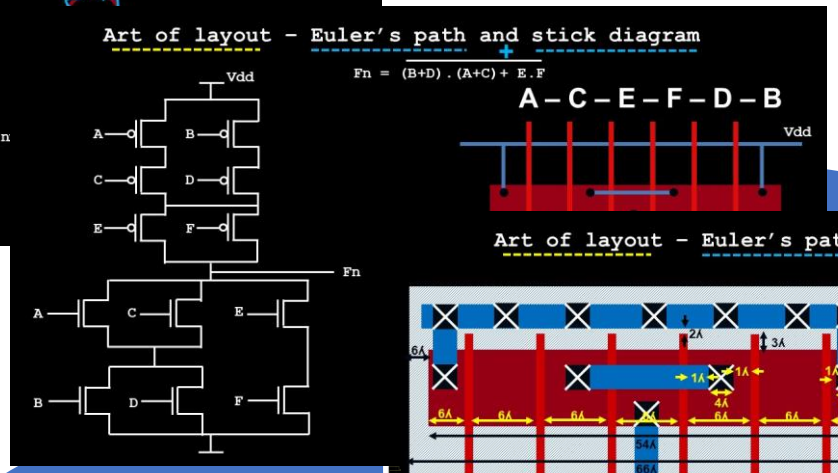


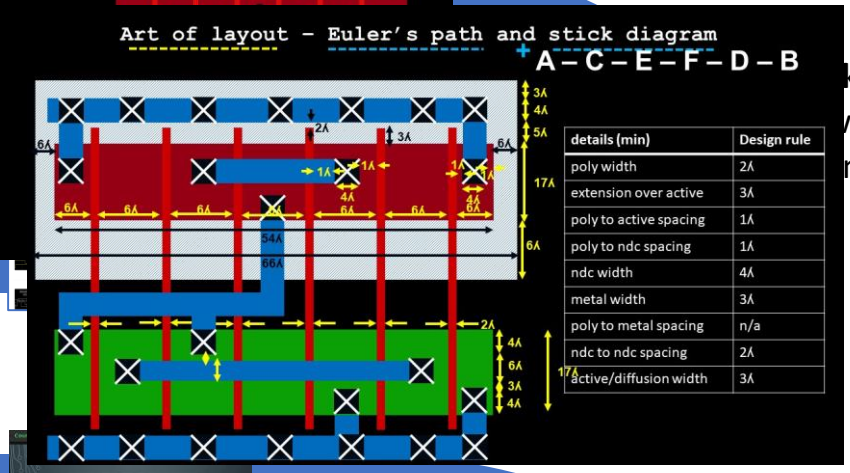


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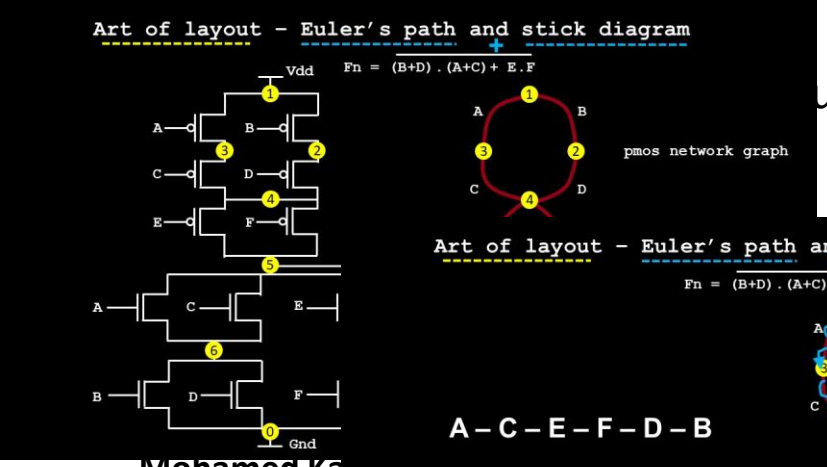


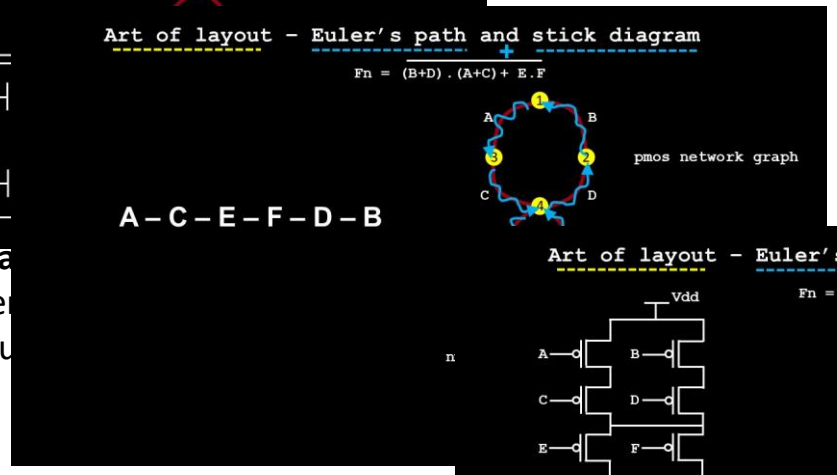


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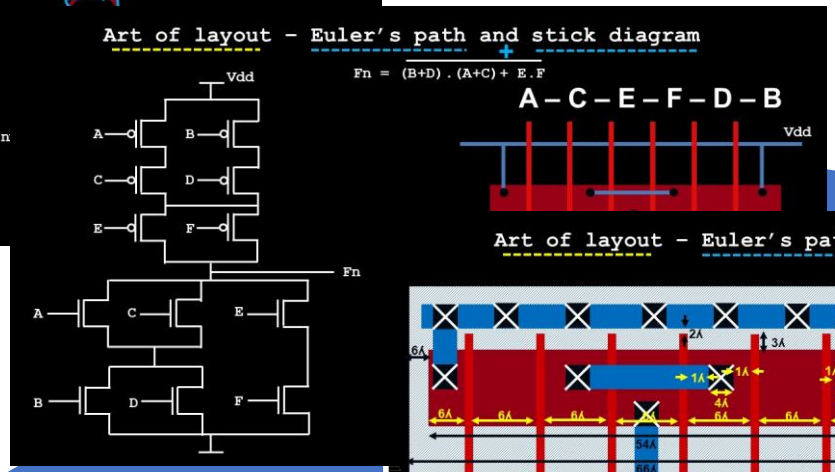


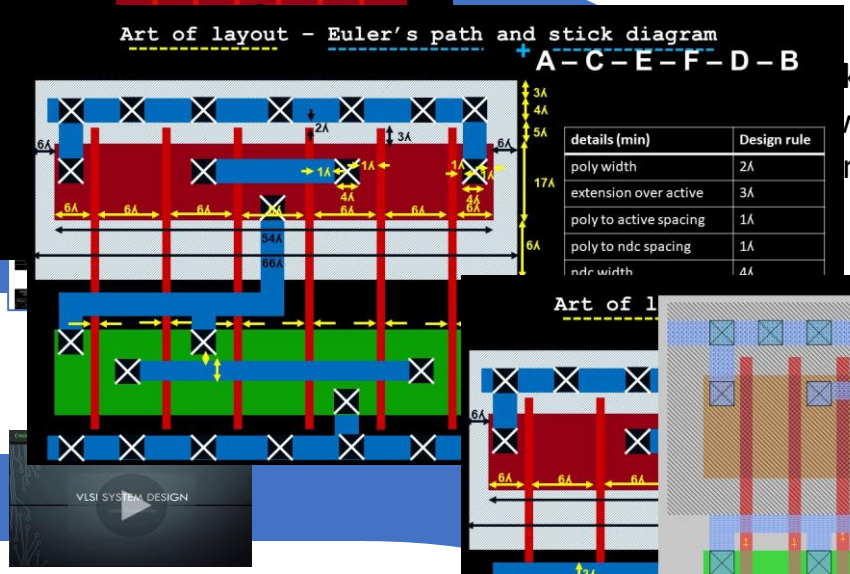


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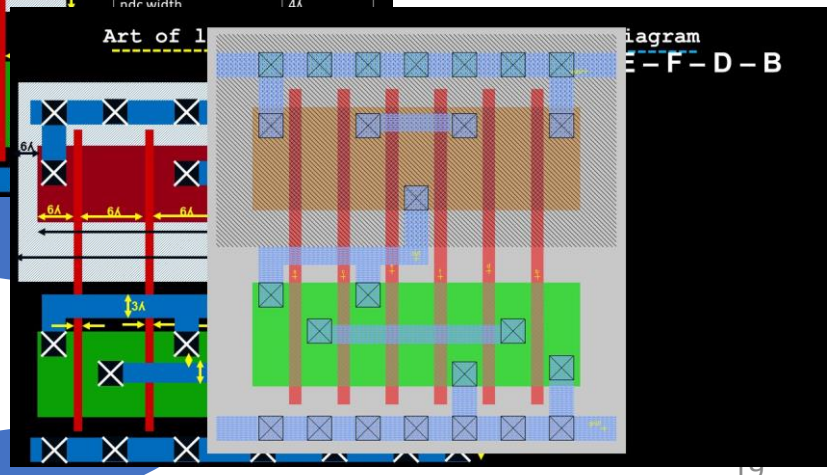


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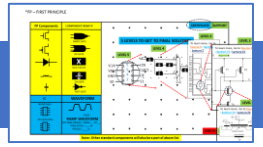

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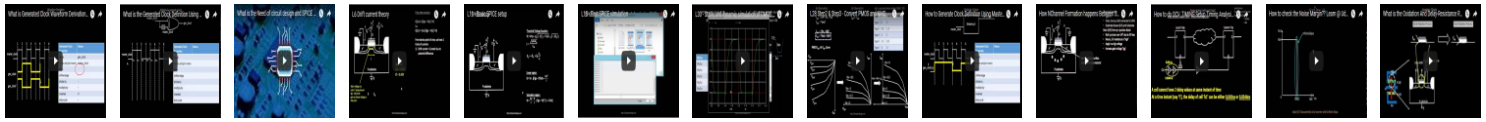

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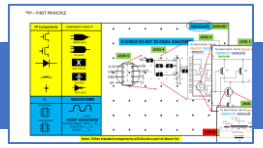

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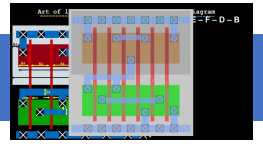

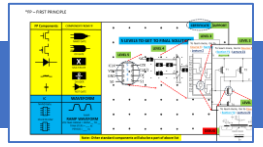

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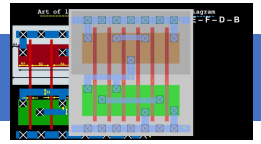

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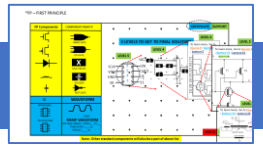

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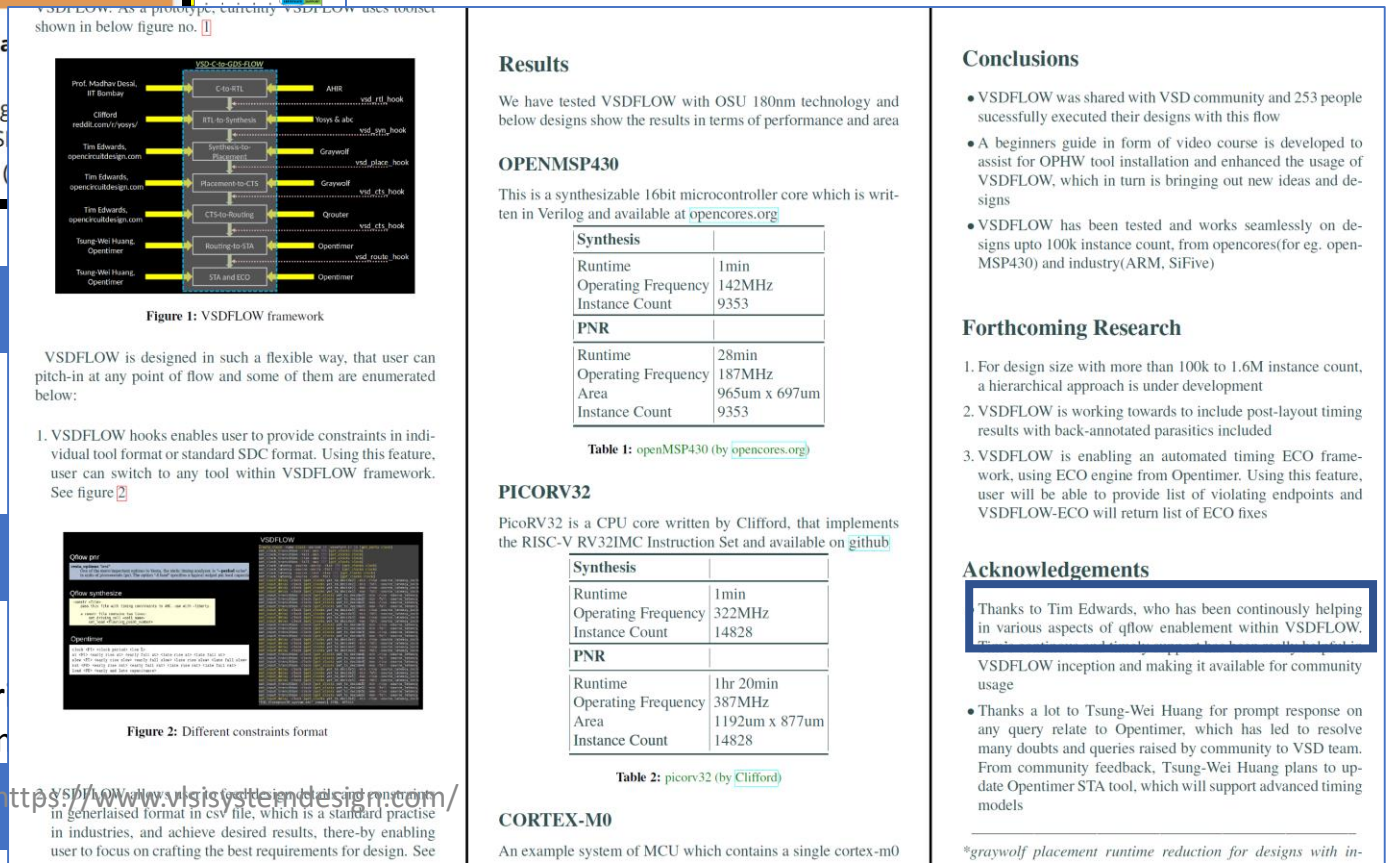

shown in below figure no. [1]




**Figure 1:** VSDFLOW framework

VSDFLOW is designed in such a flexible way, that user can pitch-in at any point of flow and some of them are enumerated below:

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in generlaised format in csv file, which is a standard practise in industries, and achieve desired results, there-by enabling user to focus on crafting the best requirements for design. See

## Results

We have tested VSDFLOW with OSU 180nm technology and below designs show the results in terms of performance and area

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This is a synthesizable 16bit microcontroller core which is written in Verilog and available at opencores.org

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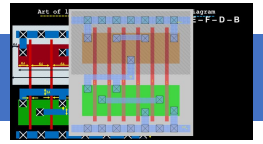

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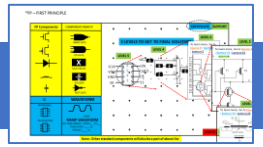

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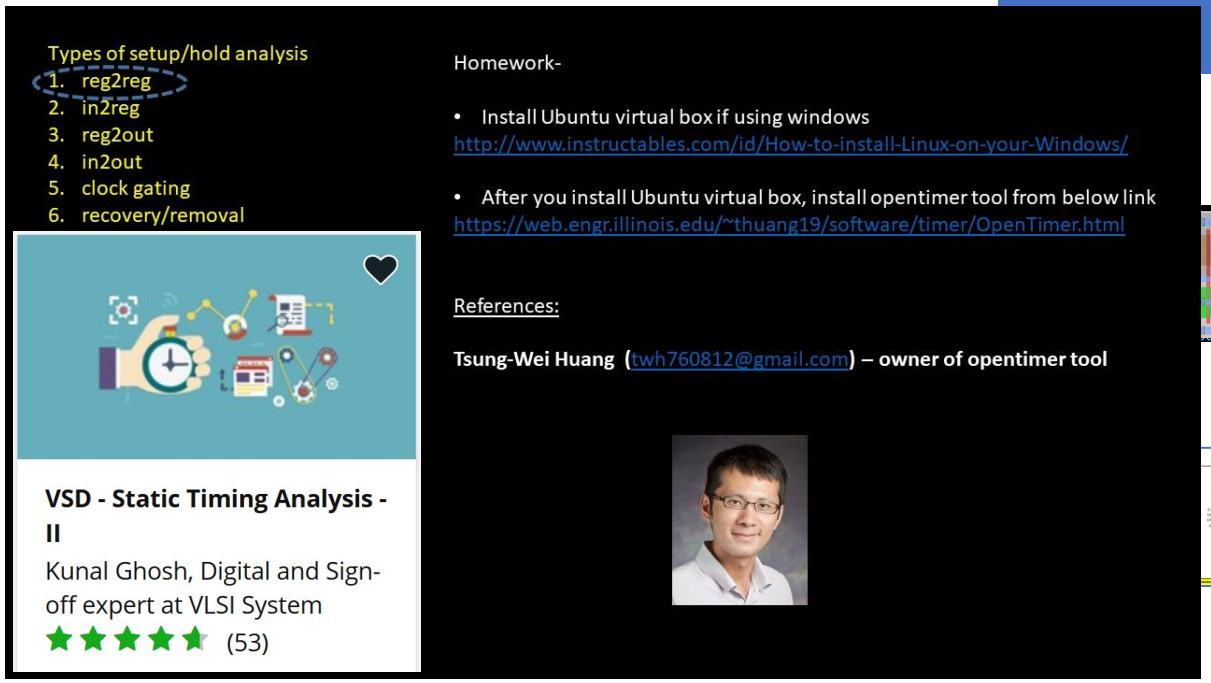


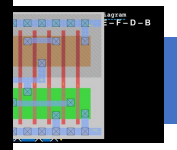

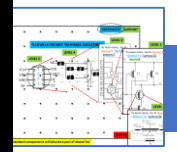

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Types of setup/hold analysis
1. reg2reg
2. in2reg
3. reg2out
4. in2out
5. clock gating
6. recovery/removal

**VSD - Static Timing Analysis - II**
Kunal Ghosh, Digital and Sign-off expert at VLSI System
★★★★½ (53)

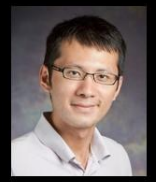
Homework-

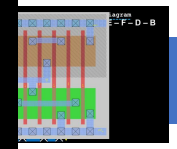
- Install Ubuntu virtual box if using windows
http://www.instructables.com/id/How-to-install-Linux-on-your-Windows/

- After you install Ubuntu virtual box, install opentimer tool from below link
https://web.engr.illinois.edu/~thuang19/software/timer/OpenTimer.html

References:

**Tsung-Wei Huang (twh760812@gmail.com) – owner of opentimer tool**





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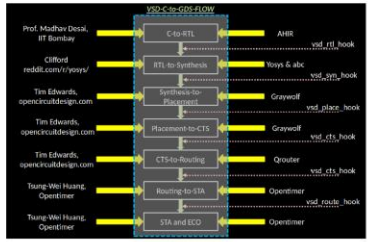


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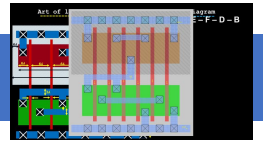

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| Recent Average Rating | Total Students | Top Student Locations | | Countries With Students |
|---|---|---|---|---|
| 4.35 | 13,015 | India | 47% | 126 |
| | | United States | 28% | |
| | | Egypt | 2% | |
| | | United Kingdom | 1% | |
| | | Canada | 1% | |

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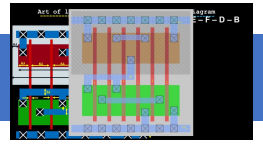

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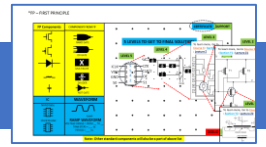

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