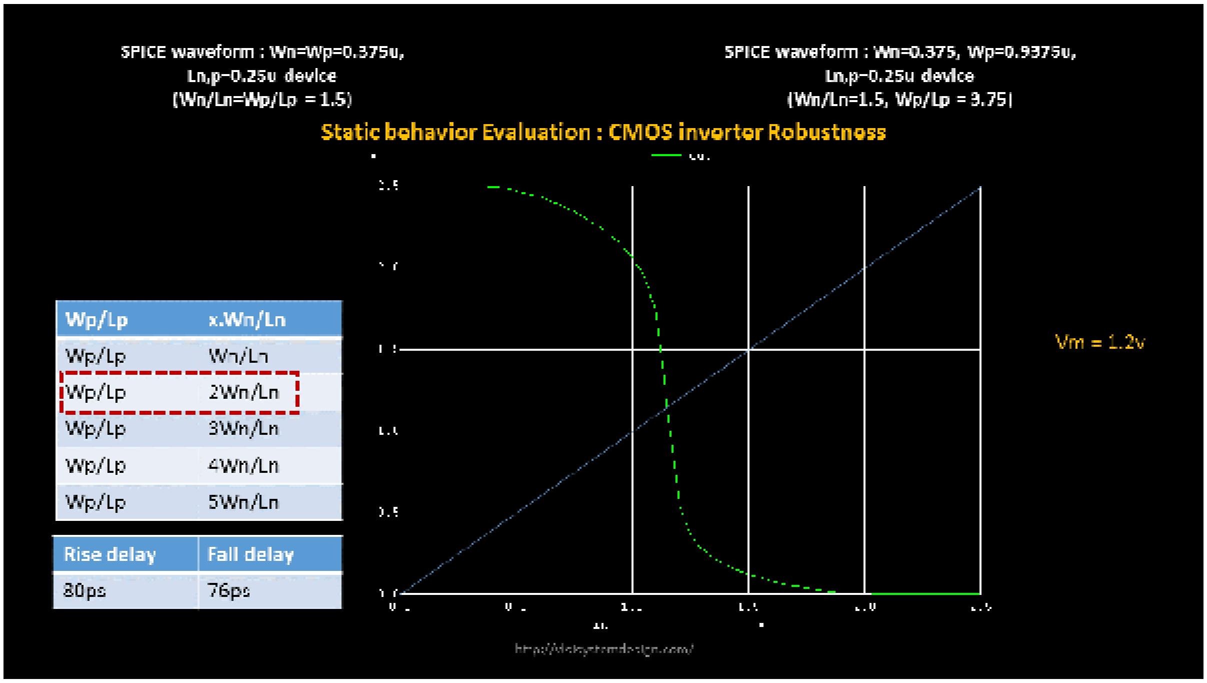
Switching threshold – Clock buffer

Kunal Ghosh

CMOS Logic so robust… I can give you 4 instances of this

1) **Vary PMOS width size to its maximum, keeping NMOS width constant and with couple of SPICE simulations**, it reveals a minimal variation on ‘**switching threshold (Vm)**’, while the functionality remains intact. Below 2 images has some SPICE simulations and numbers from experiments, I performed in my course “Circuit Design & SPICE simulations”



SPICE waveform : Wn=Wp=0.375u,
Ln,p=0.25u device
(Wn/Ln=Wp/Lp = 1.5)

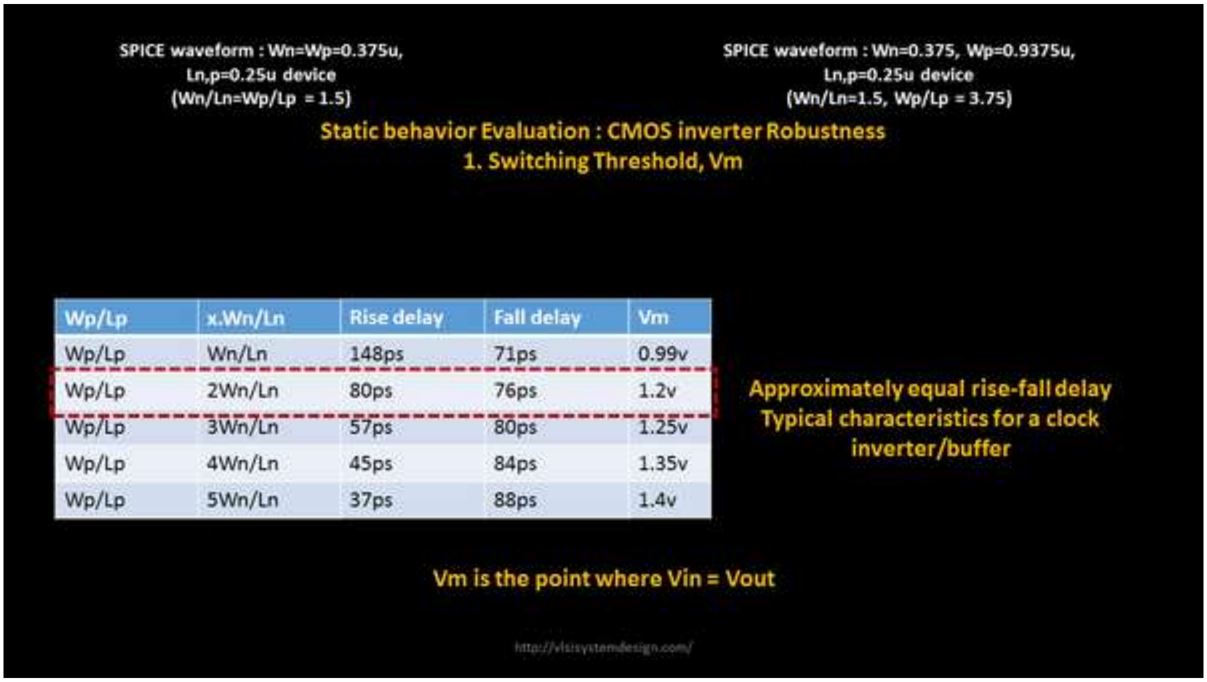
SPICE waveform : Wn=0.375, Wp=0.9375u,
Ln,p=0.25u device
(Wn/Ln=1.5, Wp/Lp = 3.75)

Static behavior Evaluation : CMOS inverter Robustness

Wp/Lp	x.Wn/Ln
Wp/Lp	Wn/Ln
Wp/Lp	2Wn/Ln
Wp/Lp	3Wn/Ln
Wp/Lp	4Wn/Ln
Wp/Lp	5Wn/Ln

Rise delay	Fall delay
80ps	76ps

Vm = 1.2v



SPICE waveform : Wn=Wp=0.375u,
Ln,p=0.25u device
(Wn/Ln=Wp/Lp = 1.5)

SPICE waveform : Wn=0.375, Wp=0.9375u,
Ln,p=0.25u device
(Wn/Ln=1.5, Wp/Lp = 3.75)

Static behavior Evaluation : CMOS inverter Robustness
1. Switching Threshold, Vm

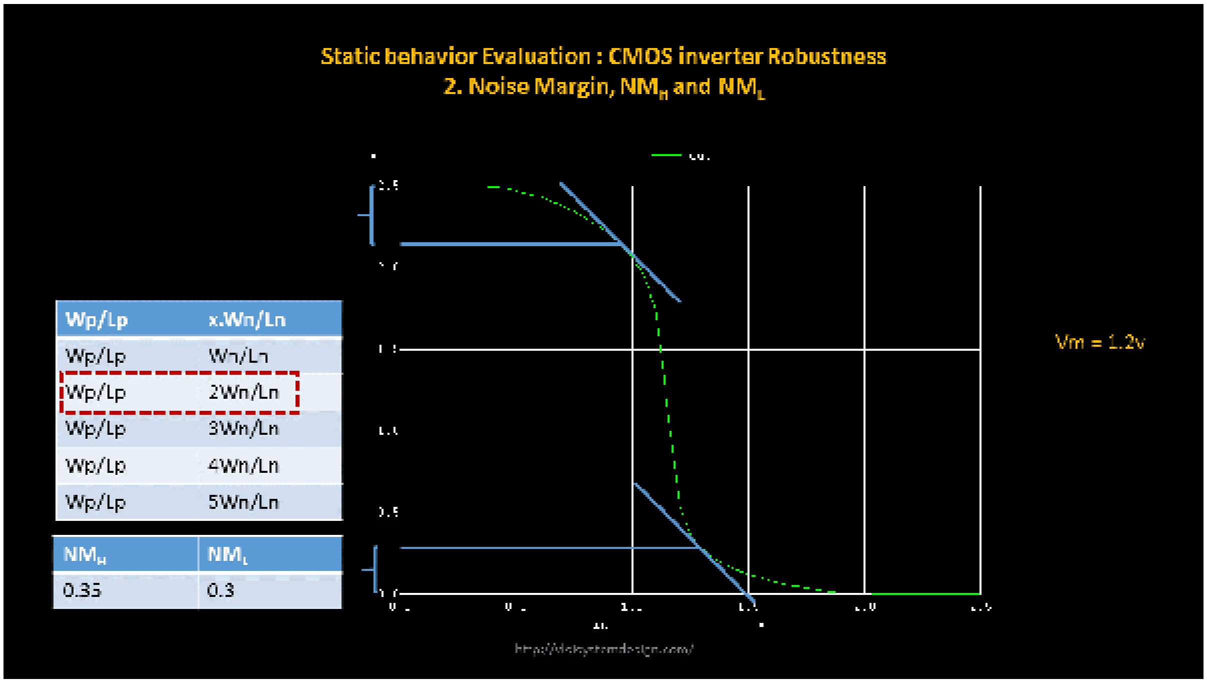
Wp/Lp	x.Wn/Ln	Rise delay	Fall delay	Vm
Wp/Lp	Wn/Ln	148ps	71ps	0.99v
Wp/Lp	2Wn/Ln	80ps	76ps	1.2v
Wp/Lp	3Wn/Ln	57ps	80ps	1.25v
Wp/Lp	4Wn/Ln	45ps	84ps	1.35v
Wp/Lp	5Wn/Ln	37ps	88ps	1.4v

Approximately equal rise-fall delay
Typical characteristics for a clock inverter/buffer

Vm is the point where Vin = Vout

http://vlsisystemdesign.com/

2) Vary PMOS width size to its maximum, keeping NMOS width constant and with couple of SPICE simulations, it’s also revealed that ‘**noise margin**’ has hardly any variation, while functionality remains intact. Watch!!!



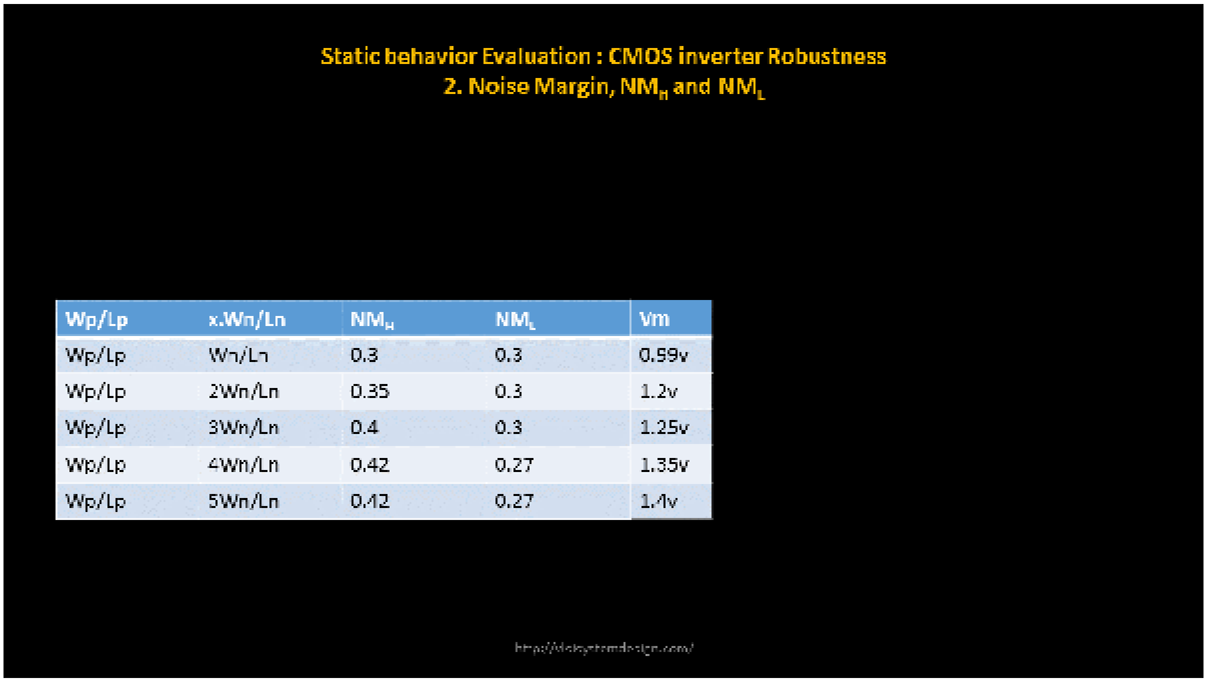
Static behavior Evaluation : CMOS inverter Robustness
2. Noise Margin, NM_H and NM_L

Wp/Lp	x.Wn/Ln
Wp/Lp	Wn/Ln
Wp/Lp	2Wn/Ln
Wp/Lp	3Wn/Ln
Wp/Lp	4Wn/Ln
Wp/Lp	5Wn/Ln

NM_H	NM_L
0.35	0.3

Vm = 1.2v

http://vlsisystemdesign.com/



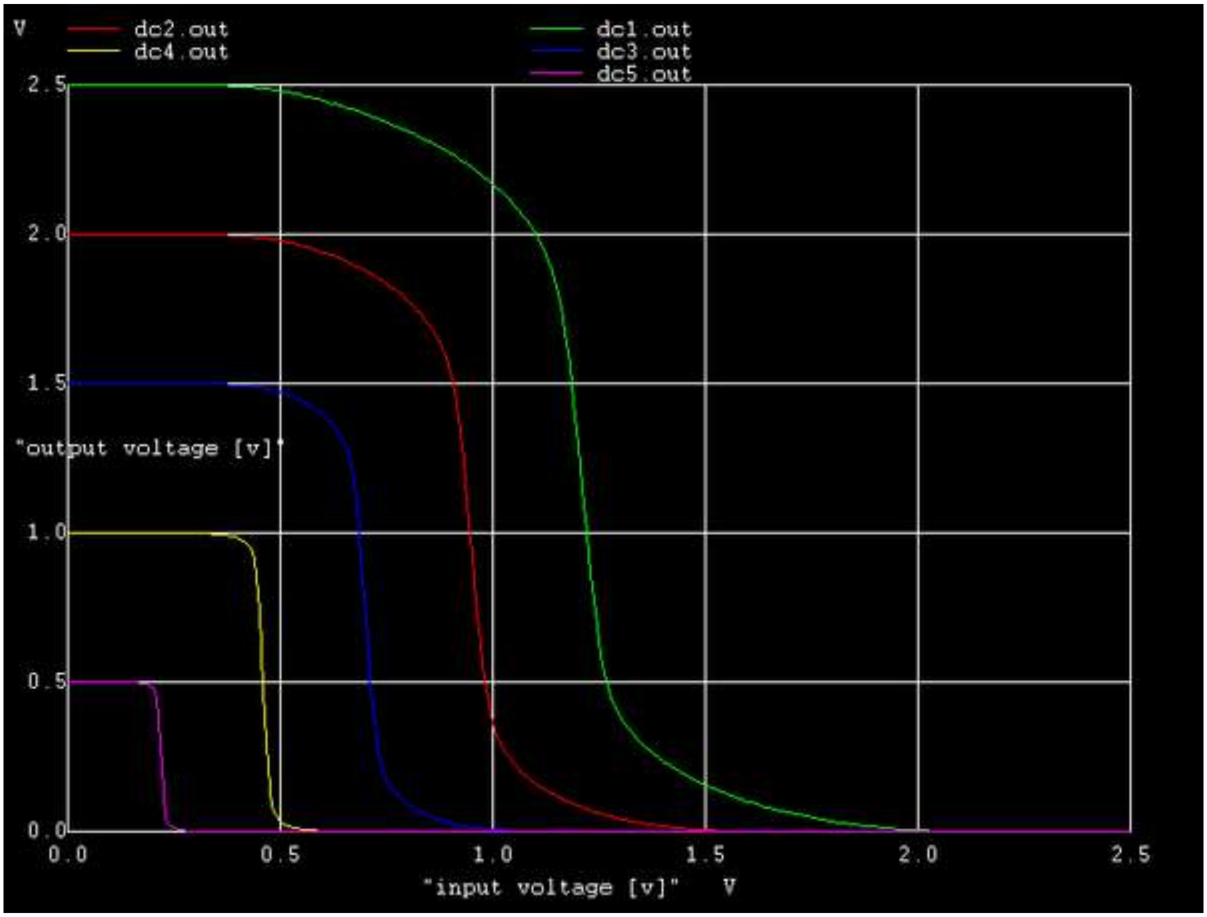
Static behavior Evaluation : CMOS inverter Robustness

2. Noise Margin, NM_H and NM_L

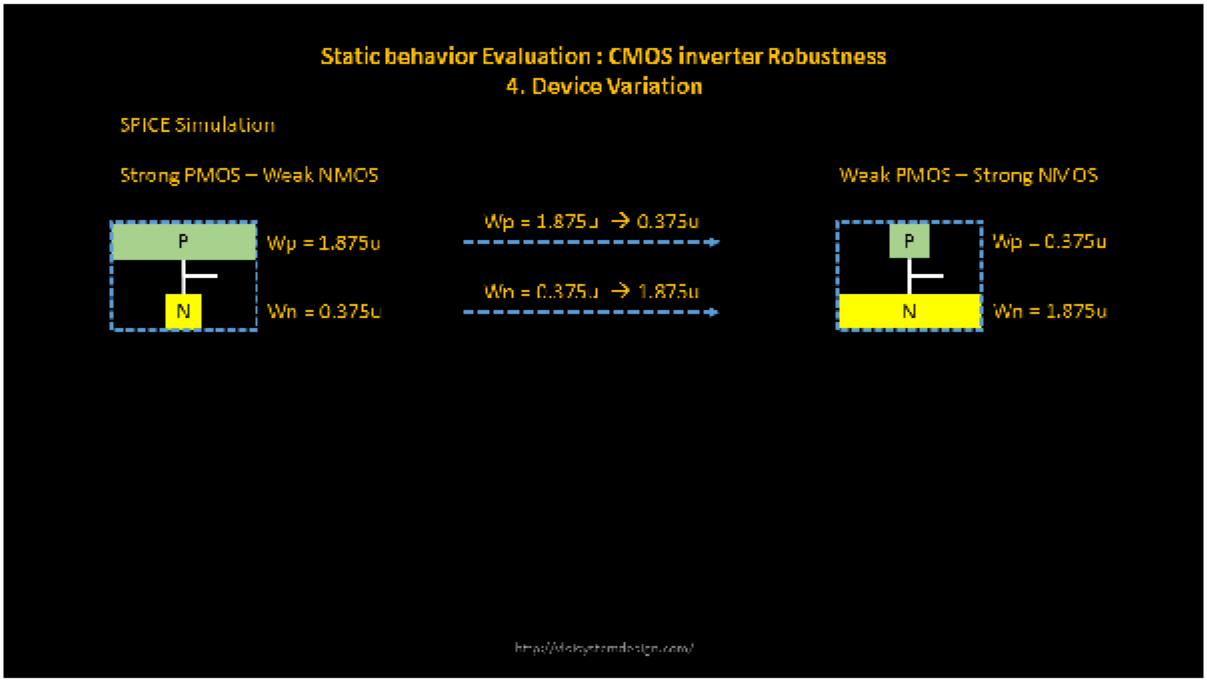
Wp/Lp	x.Wn/Ln	NM_H	NM_L	Vm
Wp/Lp	Wn/Ln	0.3	0.3	0.59v
Wp/Lp	2Wn/Ln	0.35	0.3	1.2v
Wp/Lp	3Wn/Ln	0.4	0.3	1.25v
Wp/Lp	4Wn/Ln	0.42	0.27	1.35v
Wp/Lp	5Wn/Ln	0.42	0.27	1.4v

http://vlsisystemdesign.com/

3) **Vary power supply voltage (in full range, from slightly above threshold voltage till full supply VDD), keeping NMOS/PMOS width constant, the gain improves, while functionality is still intact**. Watch!!



4) Now, vary, PMOS width from **Max to Min**, while vary NMOS width from **Min to Max** at same time, and there is very little impact in '**switching threshold'** and '**noise margin'**, while functionality is still intact. Watch!!



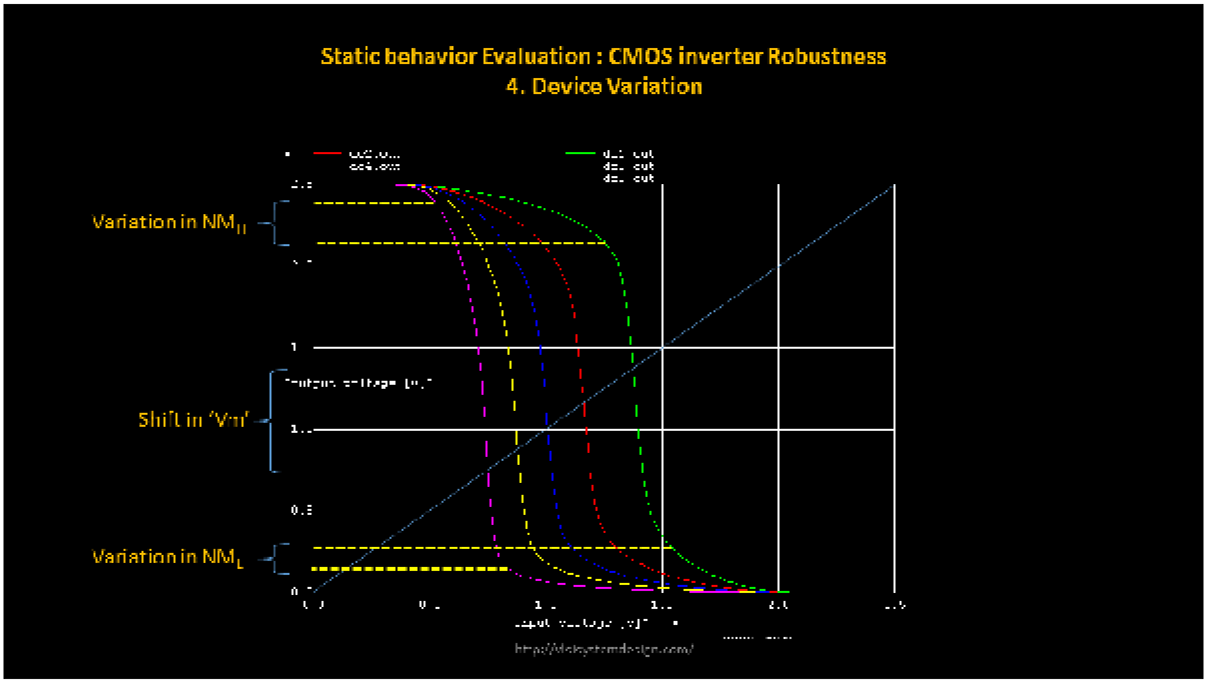
Static behavior Evaluation : CMOS inverter Robustness
4. Device Variation

SPICE Simulation

Strong PMOS – Weak NMOS

Weak PMOS – Strong NMOS

http://vlsisystemdesign.com/



Static behavior Evaluation : CMOS inverter Robustness
4. Device Variation

http://vlsisystemdesign.com/

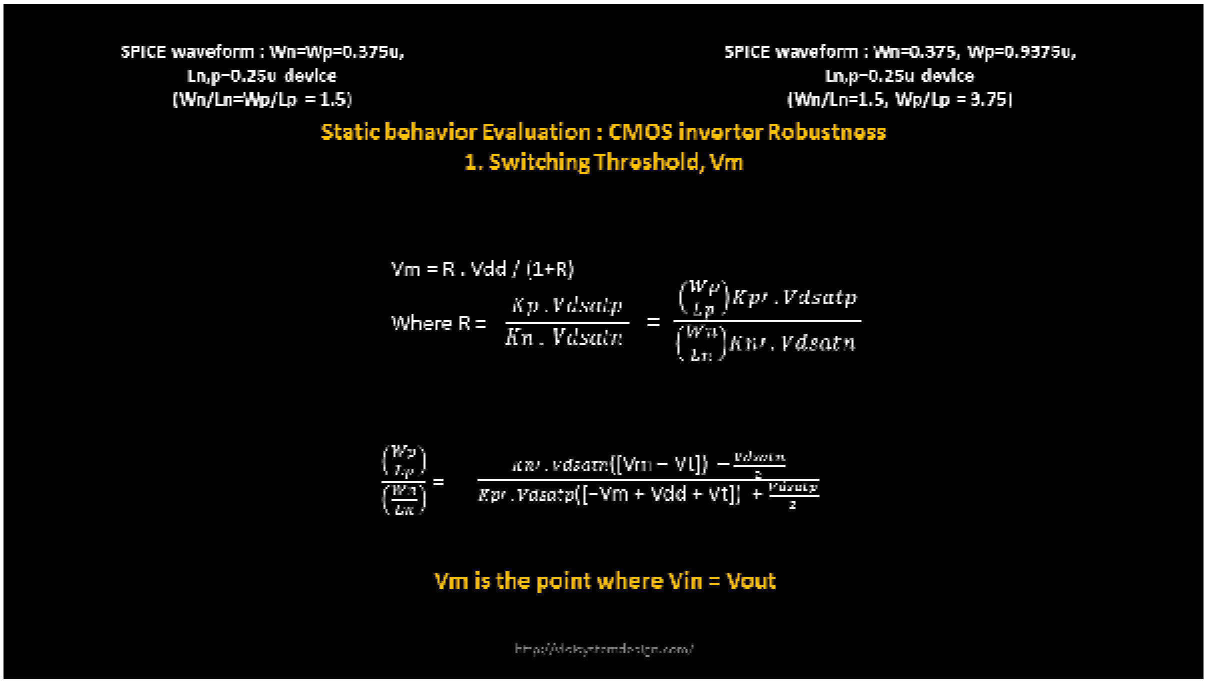
"Remember, the storm is a good opportunity for the pine and the cypress to show their strength and stability" — Ho Chi Minh

So, what is that storm, that will cause a CMOS logic to become unstable – may be a '**glitch'**. I have given enough hint for you to figure out that. Well, that would one of the key topics of my next course, when I go for dynamic simulations.

And here's more reason to be happy to discover what **defines a buffer/inverter as clock cell or regular cell**.

This is also, a common question that STA engineers have while hearing about **clock path full of clock buffers/inverters**. Well, let me try to begin to answer it over here

In last post, I talked about the robustness of CMOS logic in terms of switching threshold (i.e. a voltage at which Vin = Vout), and below table summarizes it all



SPICE waveform : Wn=Wp=0.375u,
Ln,p=0.25u device
(Wn/Ln=Wp/Lp = 1.5)

SPICE waveform : Wn=0.375, Wp=0.9375u,
Ln,p=0.25u device
(Wn/Ln=1.5, Wp/Lp = 3.75)

Static behavior Evaluation : CMOS inverter Robustness

1. Switching Threshold, Vm

Vm = R . Vdd / (1+R)

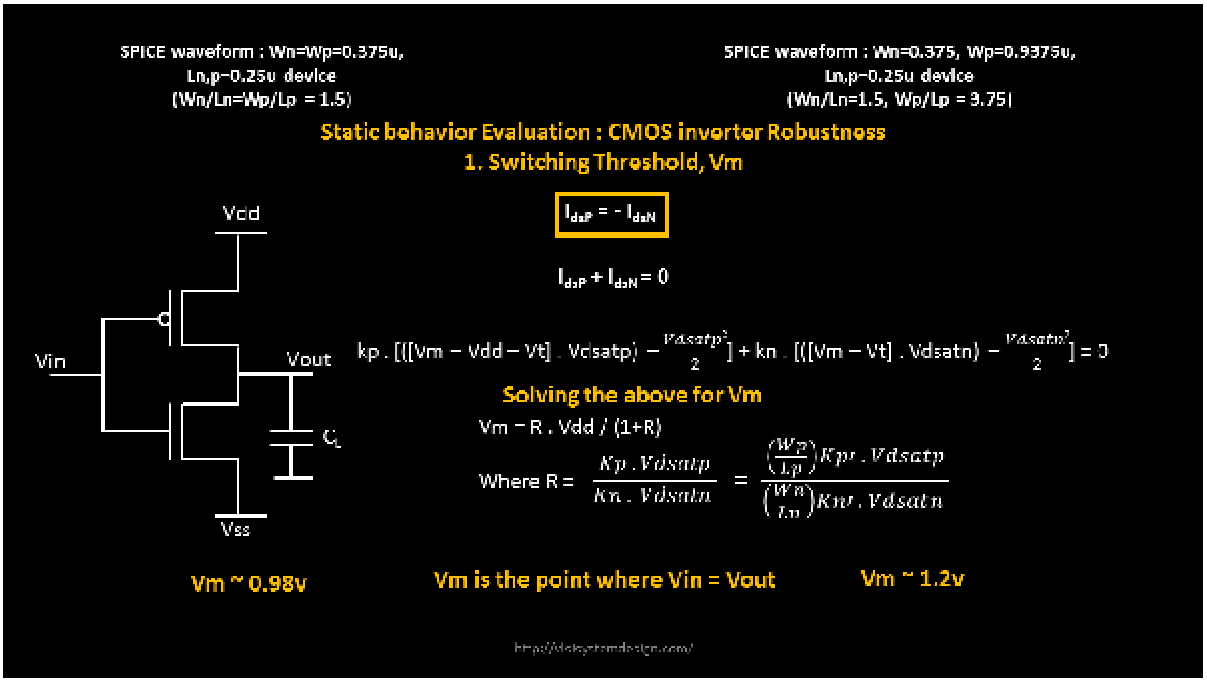
$$\text{Where R} = \frac{Kp\,.\,Vdsatp}{Kn\,.\,Vdsatn} = \frac{\left(\frac{Wp}{Lp}\right)Kp'\,.\,Vdsatp}{\left(\frac{Wn}{Ln}\right)Kn'\,.\,Vdsatn}$$

$$\frac{\left(\frac{Wp}{Lp}\right)}{\left(\frac{Wn}{Ln}\right)} = \frac{Kn'\,.\,Vdsatn([Vm - Vt]) - \frac{Vdsatn}{2}}{Kp'\,.\,Vdsatp([-Vm + Vdd + Vt]) + \frac{Vdsatp}{2}}$$

Vm is the point where Vin = Vout

http://vlsisystemdesign.com/

"On a side note" – it's always possible to hand-calculate the value of switching threshold, if you know the sizes of transistors. Below image will give a straight forward equation to do that (if it looks complex, don't worry, it has nothing to do with this post, you can safely scroll over :))



SPICE waveform : Wn=Wp=0.375u, Ln,p=0.25u device (Wn/Ln=Wp/Lp = 1.5)

SPICE waveform : Wn=0.375, Wp=0.9375u, Ln,p=0.25u device (Wn/Ln=1.5, Wp/Lp = 3.75)

Static behavior Evaluation : CMOS inverter Robustness

1. Switching Threshold, Vm

$$\boxed{I_{dsP} = - I_{dsN}}$$

$$I_{dsP} + I_{dsN} = 0$$

$$kp\,.\,[([Vm - Vdd - Vt]\,.\,Vdsatp) - \frac{Vdsatp^2}{2}] + kn\,.\,[([Vm - Vt]\,.\,Vdsatn) - \frac{Vdsatn^2}{2}] = 0$$

Solving the above for Vm

$$Vm = R\,.\,Vdd\,/\,(1+R)$$

$$\text{Where } R = \frac{Kp\,.\,Vdsatp}{Kn\,.\,Vdsatn} = \frac{\left(\frac{Wp}{Lp}\right)Kp'\,.\,Vdsatp}{\left(\frac{Wn}{Ln}\right)Kn'\,.\,Vdsatn}$$

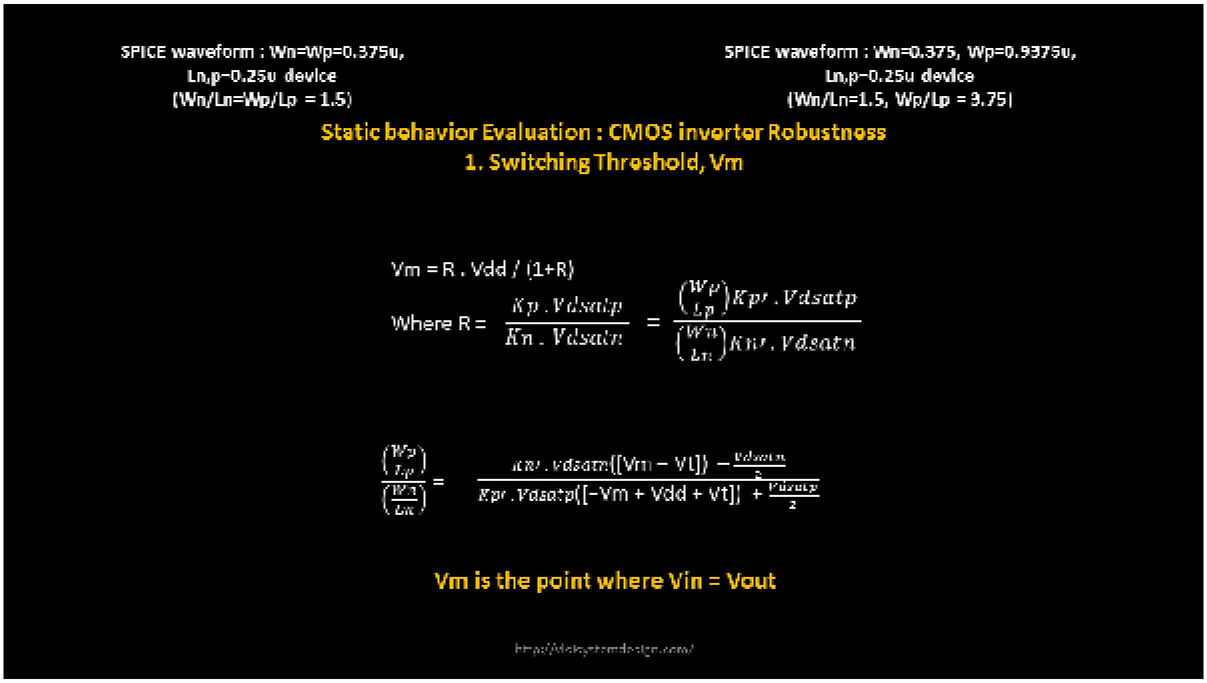
Vm ~ 0.98v

Vm is the point where Vin = Vout

Vm ~ 1.2v

http://vlsisystemdesign.com/

Alternatively, if you want to **design your CMOS inverter around certain switching threshold**, you can do that as well. Below equation will help to obtain the same (Again, if you do not follow this equation, just scroll over:), you can always learn about it in my Circuit design course)



SPICE waveform : Wn=Wp=0.375u, Ln,p=0.25u device (Wn/Ln=Wp/Lp = 1.5)

SPICE waveform : Wn=0.375, Wp=0.9375u, Ln,p=0.25u device (Wn/Ln=1.5, Wp/Lp = 3.75)

Static behavior Evaluation : CMOS inverter Robustness

1. Switching Threshold, Vm

$$Vm = R\,.\,Vdd\,/\,(1+R)$$

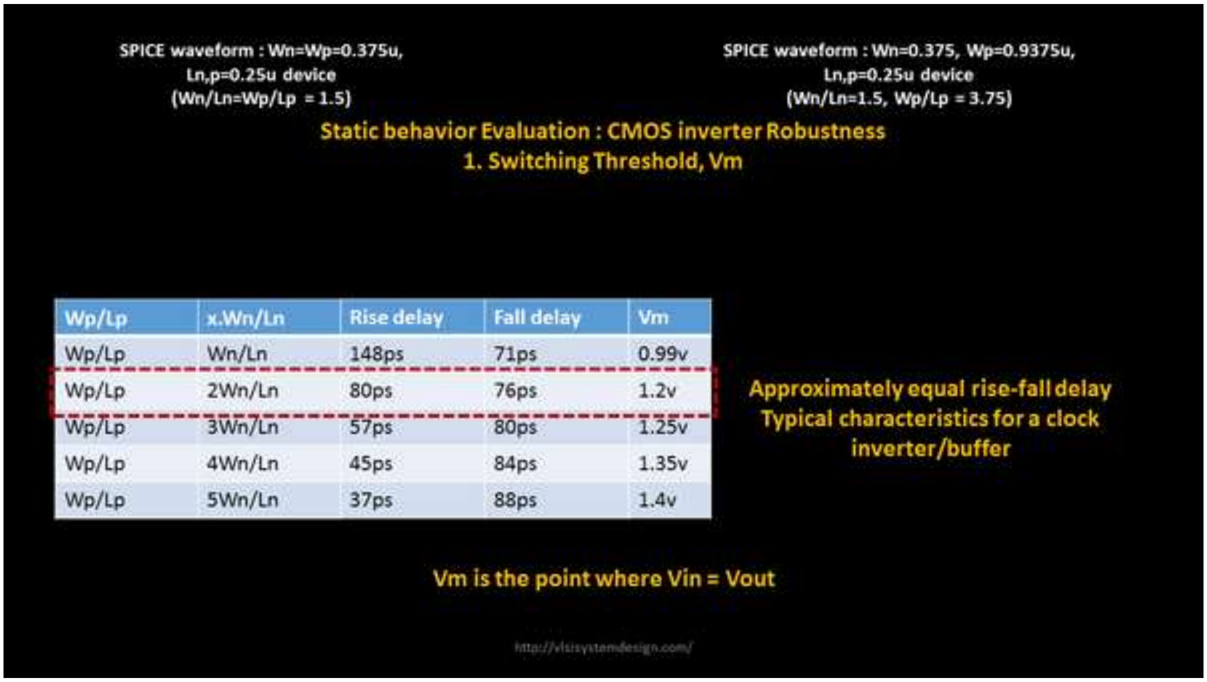
$$\text{Where } R = \frac{Kp\,.\,Vdsatp}{Kn\,.\,Vdsatn} = \frac{\left(\frac{Wp}{Lp}\right)Kp'\,.\,Vdsatp}{\left(\frac{Wn}{Ln}\right)Kn'\,.\,Vdsatn}$$

$$\frac{\left(\frac{Wp}{Lp}\right)}{\left(\frac{Wn}{Ln}\right)} = \frac{Kn'\,.\,Vdsatn([Vm - Vt]) - \frac{Vdsatn}{2}}{Kp'\,.\,Vdsatp([-Vm + Vdd + Vt]) + \frac{Vdsatp}{2}}$$

Vm is the point where Vin = Vout

http://vlsisystemdesign.com/

Moving on … If you observe the below table, you will find out, that **if PMOS is twice the NMOS in a CMOS inverter**, you get the switching threshold close to middle of your supply voltage, and you also get a **benefit of equal rise-fall time of that inverter.** Same logic applies for buffer as well



SPICE waveform : Wn=Wp=0.375u,
Ln,p=0.25u device
(Wn/Ln=Wp/Lp = 1.5)

SPICE waveform : Wn=0.375, Wp=0.9375u,
Ln,p=0.25u device
(Wn/Ln=1.5, Wp/Lp = 3.75)

Static behavior Evaluation : CMOS inverter Robustness
1. Switching Threshold, Vm

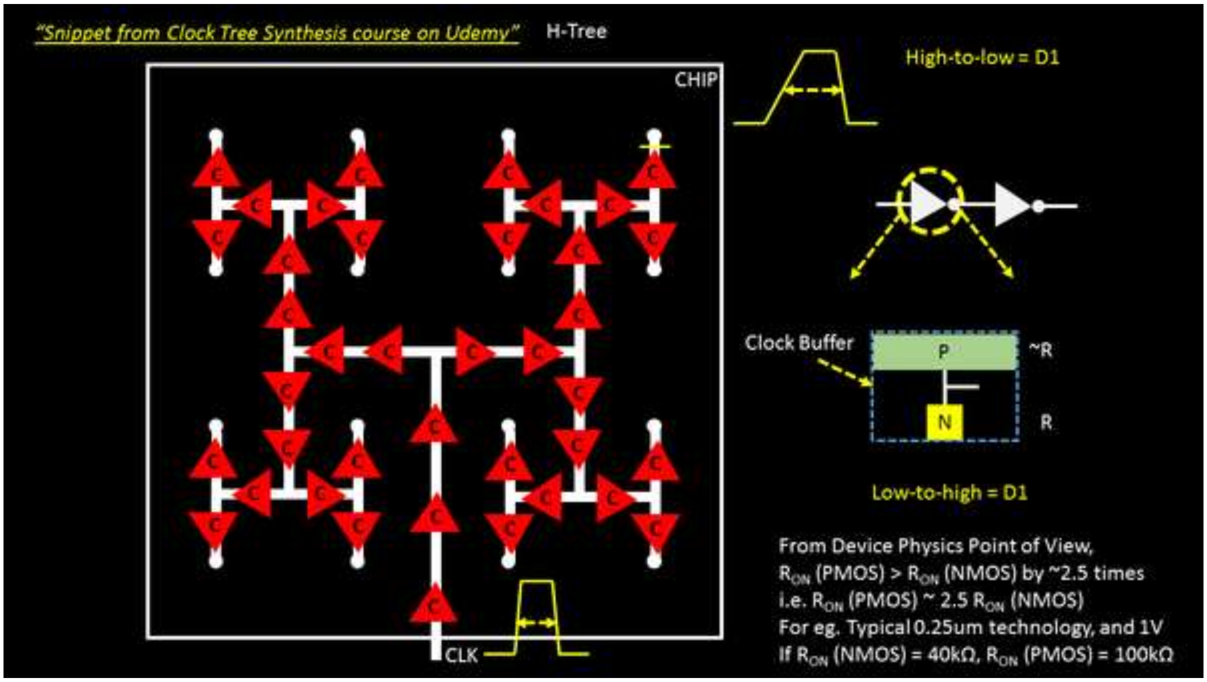
Wp/Lp	x.Wn/Ln	Rise delay	Fall delay	Vm
Wp/Lp	Wn/Ln	148ps	71ps	0.99v
Wp/Lp	2Wn/Ln	80ps	76ps	1.2v
Wp/Lp	3Wn/Ln	57ps	80ps	1.25v
Wp/Lp	4Wn/Ln	45ps	84ps	1.35v
Wp/Lp	5Wn/Ln	37ps	88ps	1.4v

Approximately equal rise-fall delay
Typical characteristics for a clock
inverter/buffer

Vm is the point where Vin = Vout

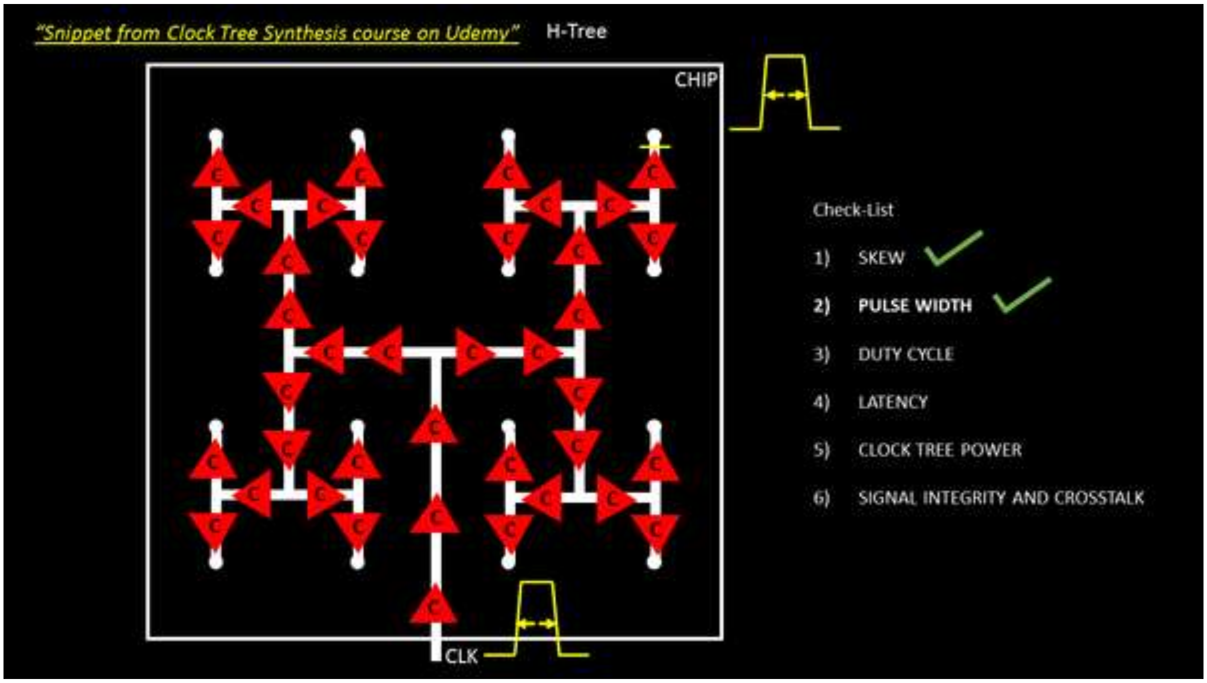
http://vlsisystemdesign.com/

If you recollect the below image from my clock tree synthesis course, where the clock signal from clock port got disturbed at flop clock pin



From Device Physics Point of View,
R_{ON} (PMOS) > R_{ON} (NMOS) by ~2.5 times
i.e. R_{ON} (PMOS) ~ 2.5 R_{ON} (NMOS)
For eg. Typical 0.25um technology, and 1V
If R_{ON} (NMOS) = 40kΩ, R_{ON} (PMOS) = 100kΩ

I had solved this problem using **a clock cell, whose rise-fall delay was exactly** (or approximately) the same



Check-List

1) SKEW ✓
2) **PULSE WIDTH** ✓
3) DUTY CYCLE
4) LATENCY
5) CLOCK TREE POWER
6) SIGNAL INTEGRITY AND CROSSTALK