Signal integrity (SI-glitch)

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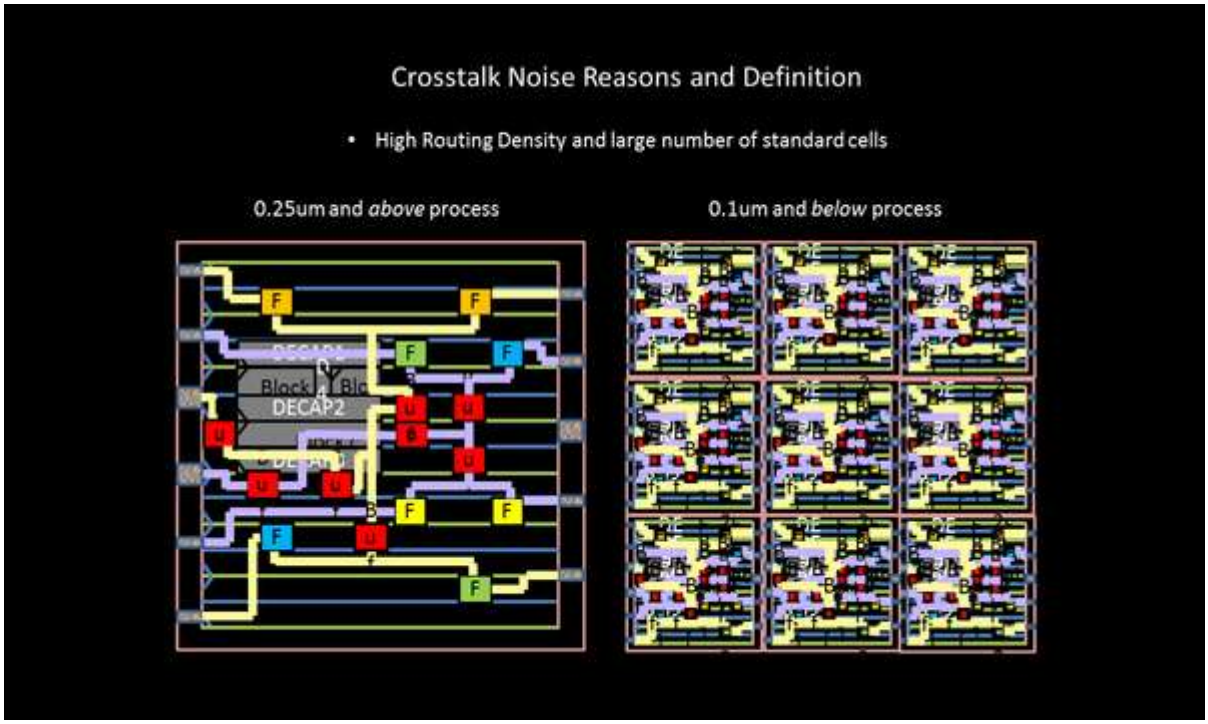
Let me start this with a 30-sec video

https://youtu.be/P1hYe7kzcag

Well …. That's glitch … Plain and simple!!!

Ahhh…. It's a pain … right!! I can tell you exactly, why the above happens. Stay with me!!

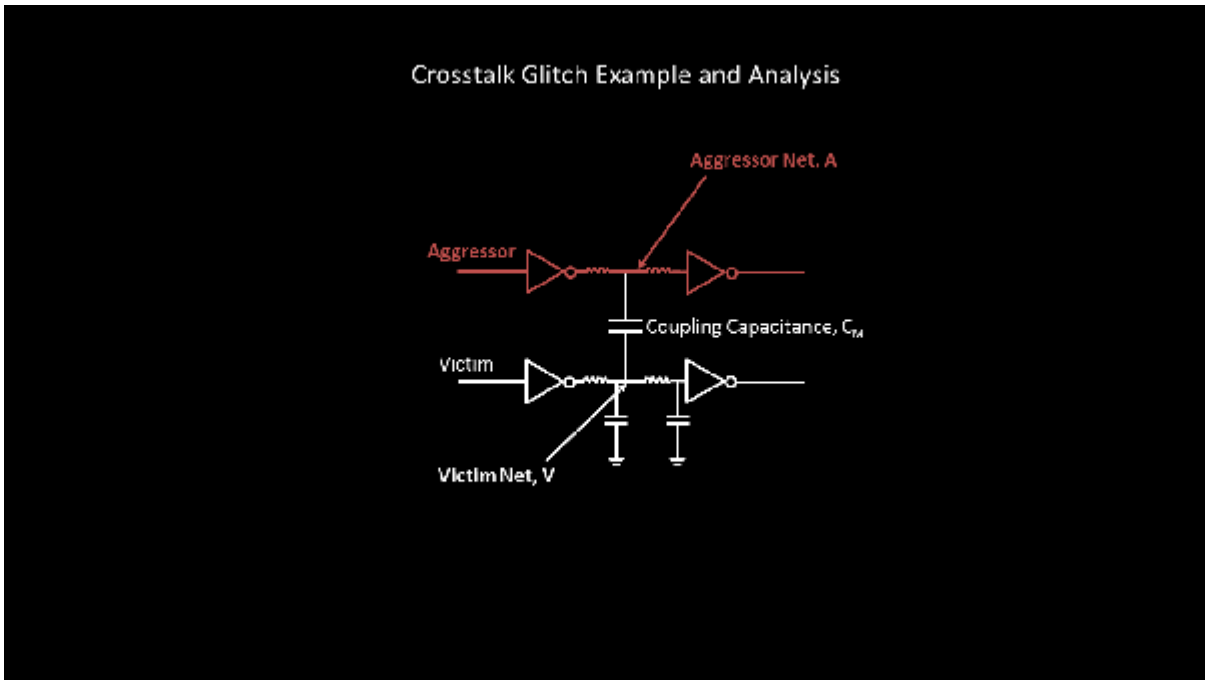
On a circuit, fabricated on silicon, there are trillions of wires packed in a small area**,** something like below, and as me and you demand for higher speed and huge number of applications, poor engineers [:(] try to pack even more devices and wires in that tiny area



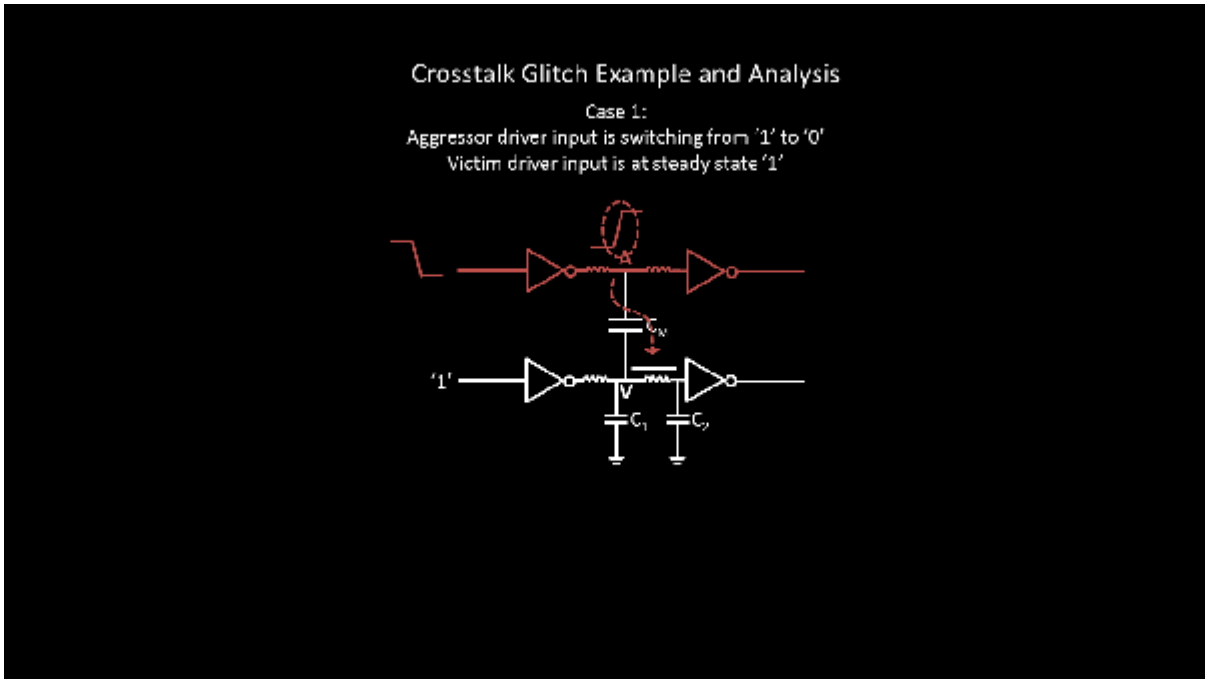
Imagine a situation, where, in a room of size of about 20 people, you put 50 people, and all 50 people talk!!

No 2 people can have a meaningful conversation, as they will be disturbed by what others are talking. Now put the below little 2 wires into the above situation and, imagine what the wires go through. They interfere with each other, through the coupling capacitor.

The stronger wire, is given the name "Aggressor (A)" and the weaker wire is given the name "Victim (V)".



Let's take a case, where 'A' switches and 'V' is silent, like below

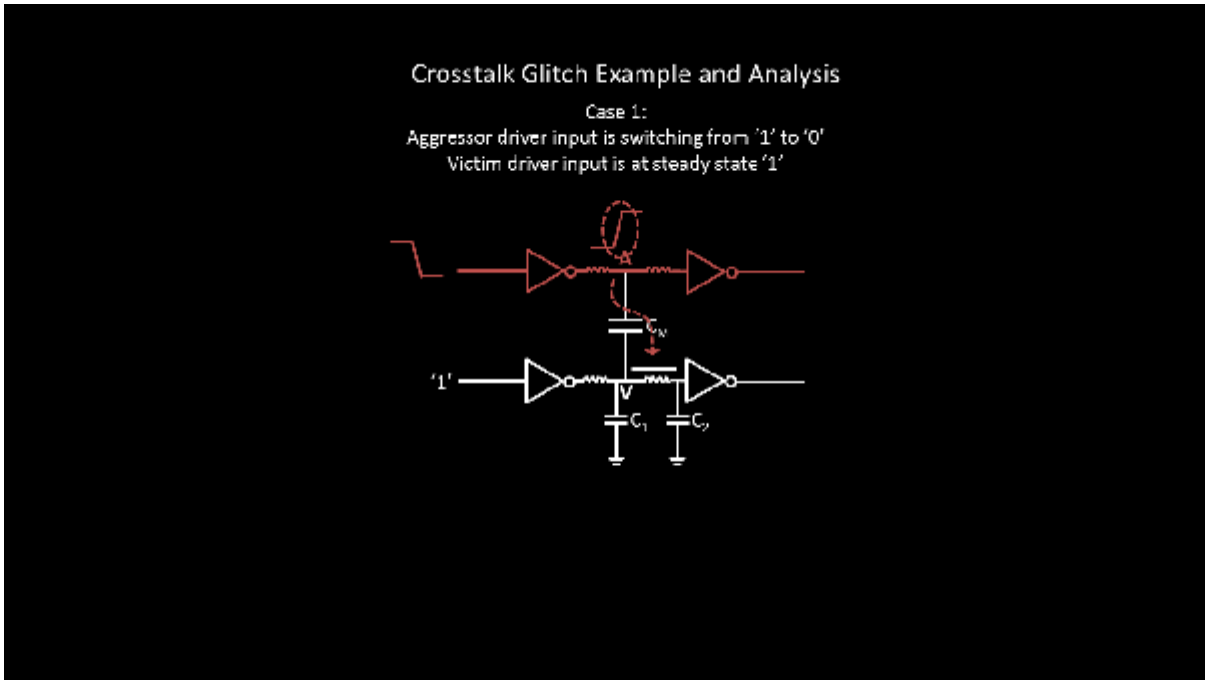


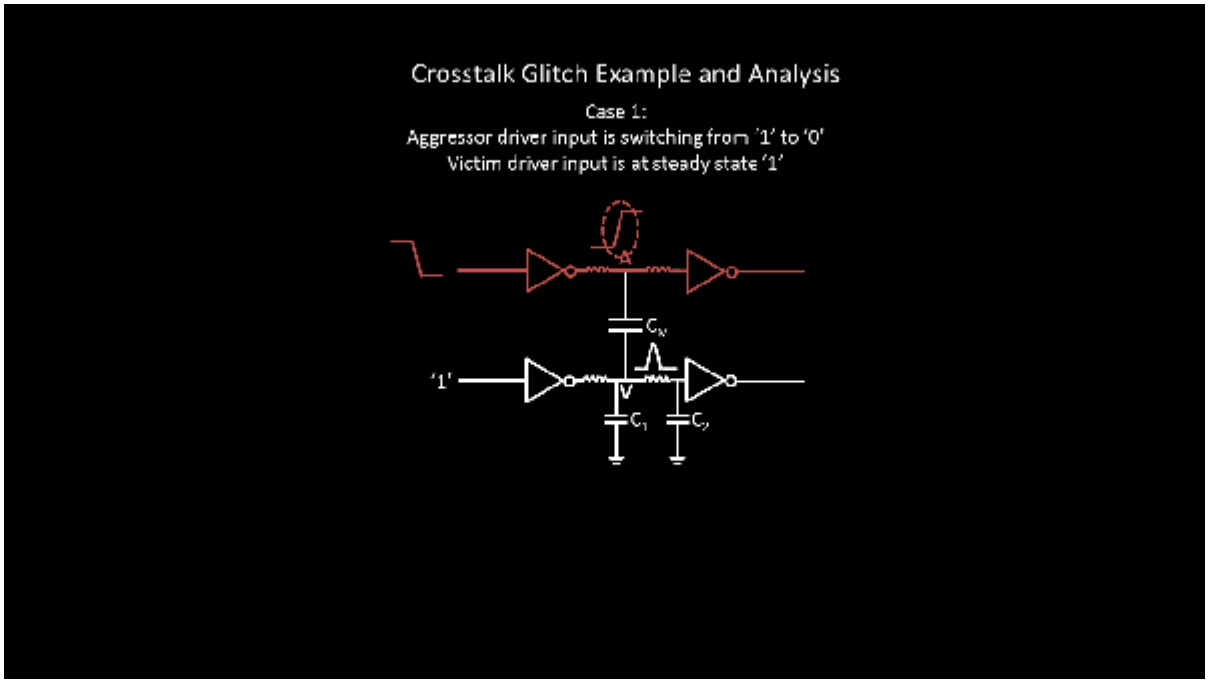
When we say, "rise transition", it means, we are charging some capacitance, and the amount of charge the capacitance has, decides its logic value.

A fully charged capacitor, will be called 'logic 1' and an empty or discharged capacitor will be called 'logic 0'. Unfortunately, the wires here are so close, that there is another capacitance between them, and along with charges

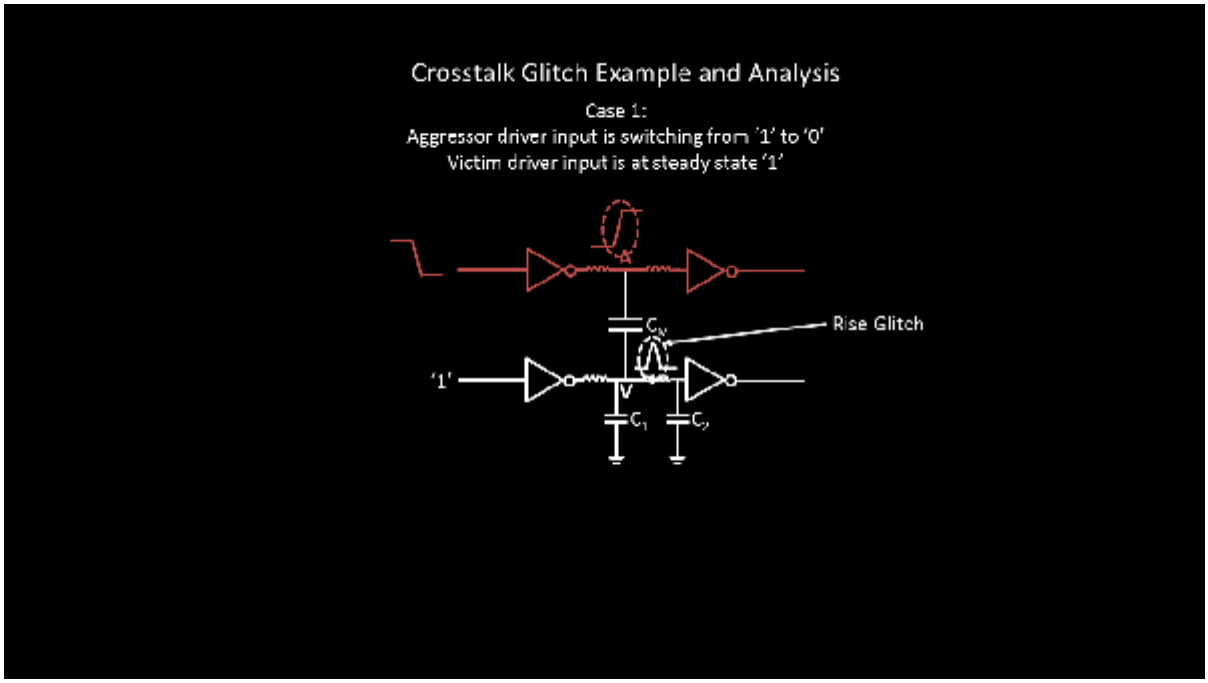
on C1 and C2, the amount of charge on Cm will also play a crucial role in deciding whether ‘V’ is at logic ‘1’ or ‘0’.

And that’s exactly what happens. The rising transition of ‘A’, charges Cm to such a level, that, for a moment, at ‘V’, the voltage rises**.**

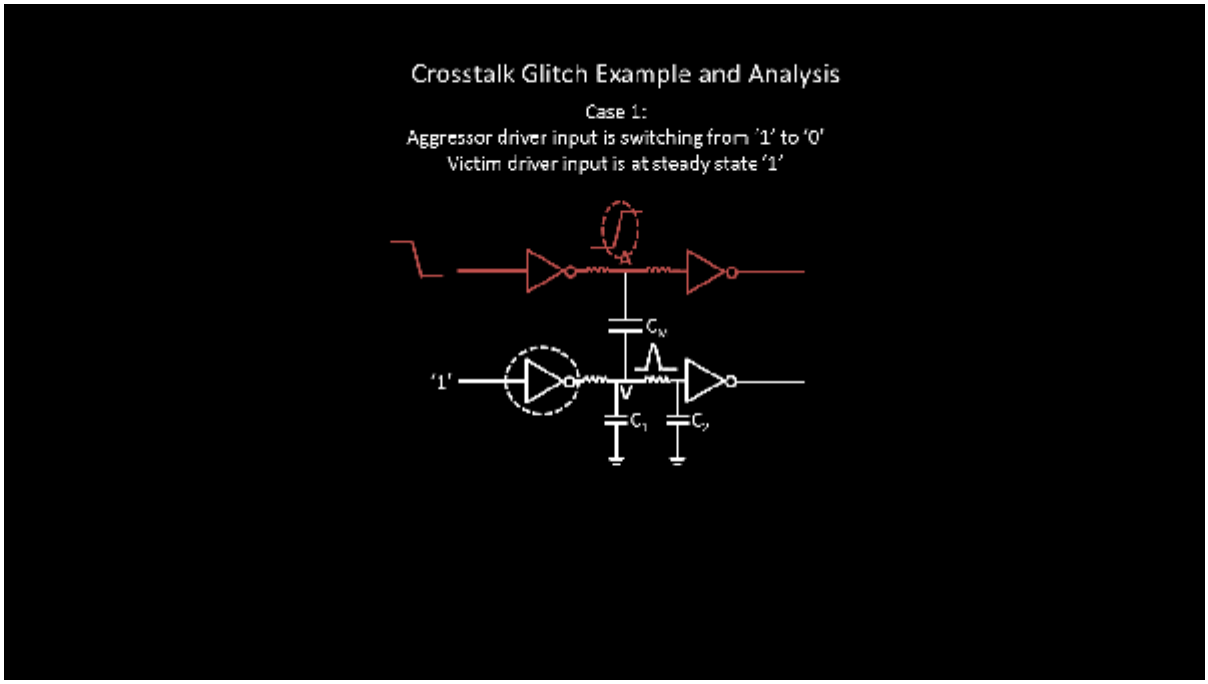




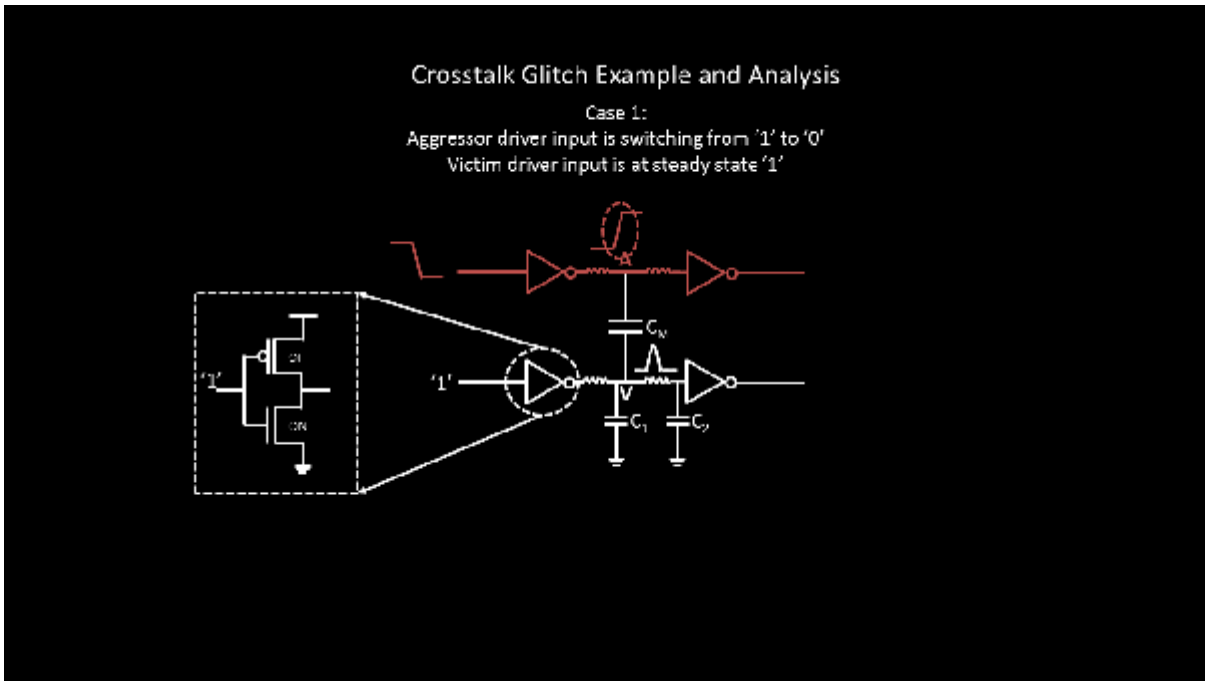
And this is called a ‘rise glitch **‘.** This glitch can be so strong, that it might just change the functionality of the system**, a**nd I will come back on this in my next post. You know what!!



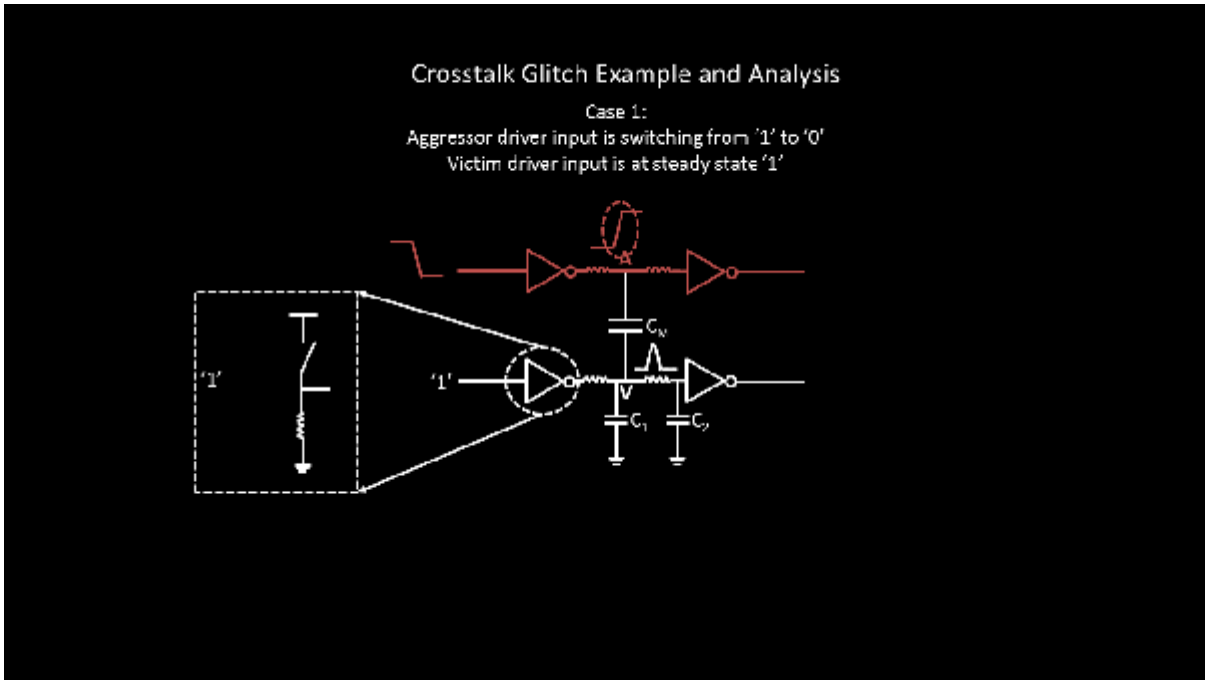
The big question… Is this glitch harmful or will it die out as it progresses through the next inverter connected to it? Let’s come back to this question in some time. For now, let’s analyze this glitch even more. Let’s see, if there’s any catch. Let’s do some smart work here. Have a close look at the inverter just before this glitch



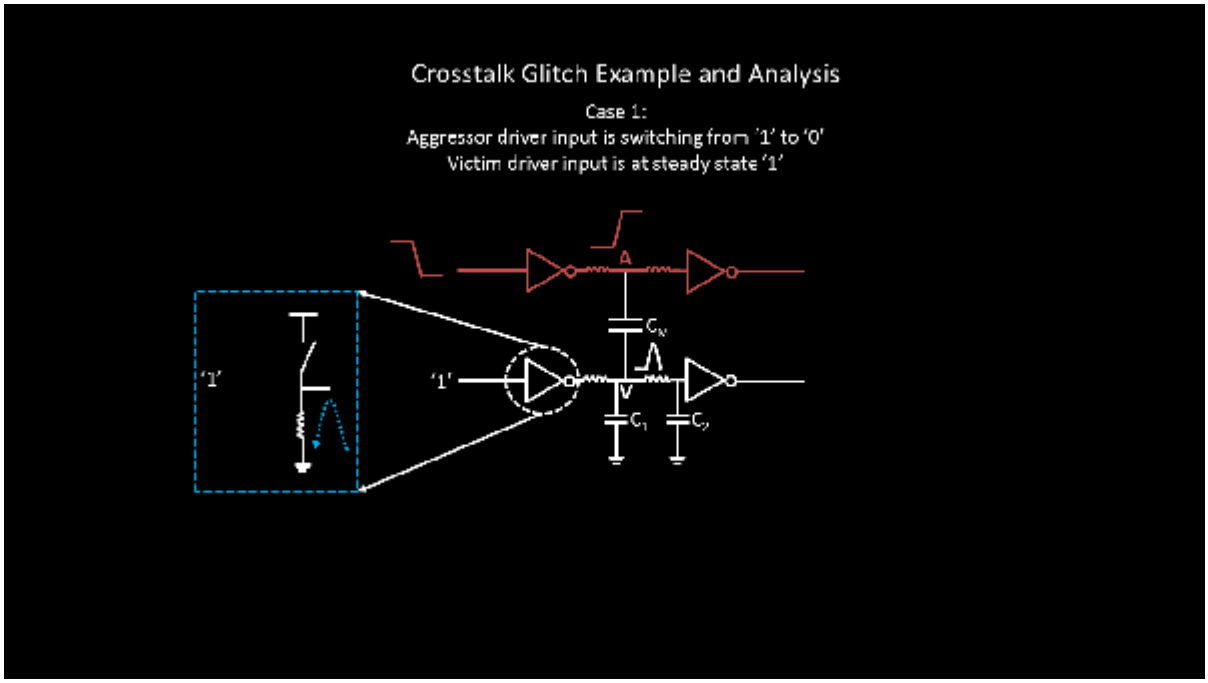
And derive the current position of the inverter below, using PMOS/NMOS/Resistance/Capacitance. (I really love to go to that deep level). Also, very soon, after you go through all my online lectures/posts, you will realize, its these MOSFET's and its internal resistances and capacitance, that build the ***$Billion*** VLSI world and drive VLSI industries

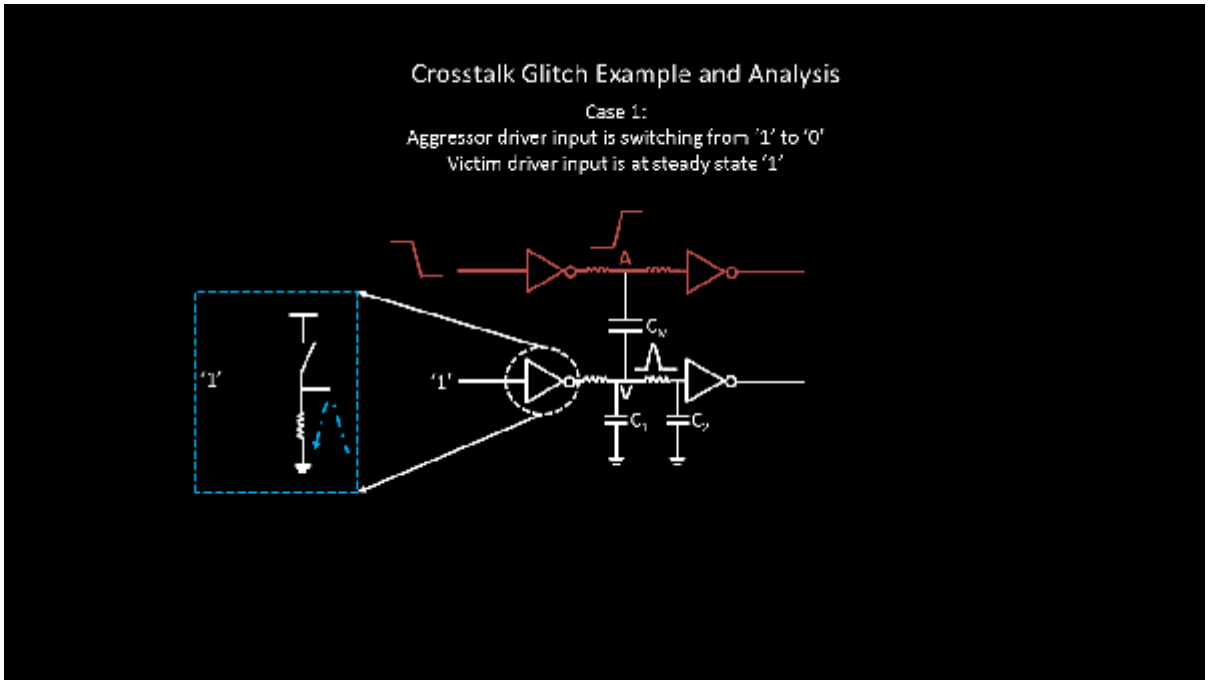


The off PMOS can be replaced by an open switch and on NMOS can be replaced by a resistance like below

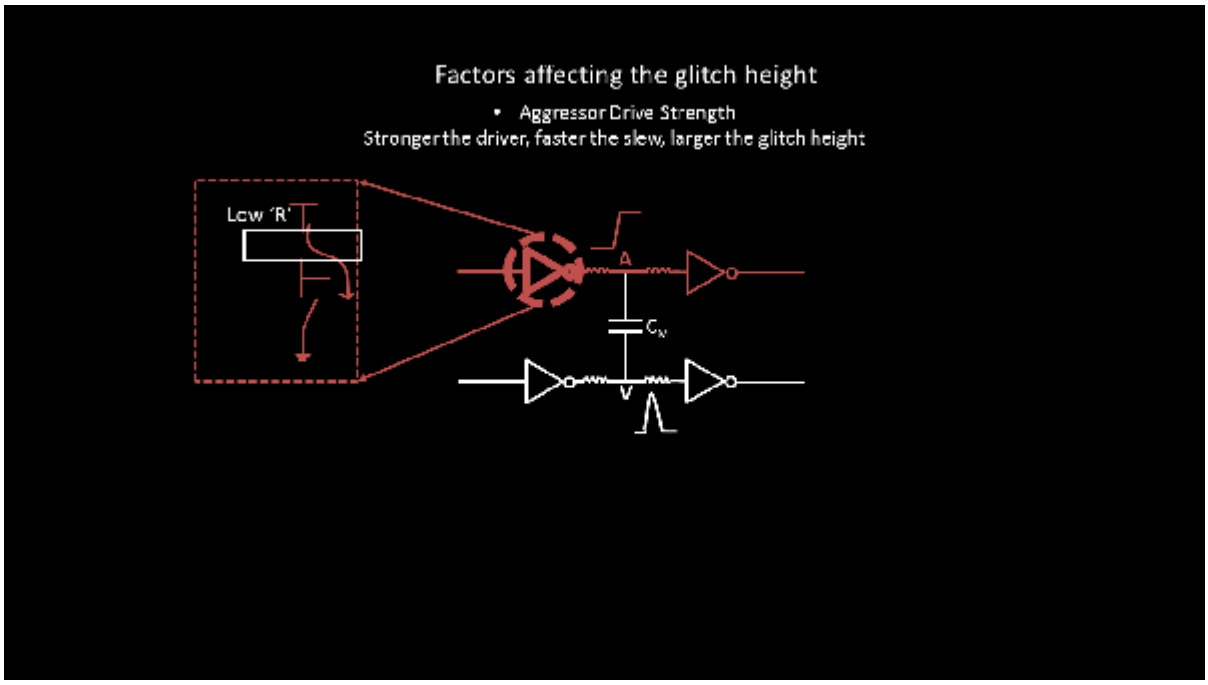


In a situation like this, a glitch becomes an issue, if the inverter is not able to completely discharge the extra ‘charge’ deposited by the aggressor.
The below 2 images will help to explain the same





In the above case, the inverter (NMOS specifically) could discharge the glitch completely, thus making this one as a ‘safe glitch’. And just now, I introduced you to 2 new things …. 1) a way to reduce glitch, and 2) the term ‘safe glitch’.



In this one, I have represented resistance by a box. Wider the box, least is the resistance, more area available for current to flow from supply to output load, and hence faster it will charge the output load.

Did you notice one thing? Due to wide box, these kinds of transistors are larger in size, and hence occupy lot of area on chip.

Also, the impact of having these kind of devices as the aggressor, makes 'A' so strong that it can charge the coupling cap very fast, thus producing the maximum glitch height.

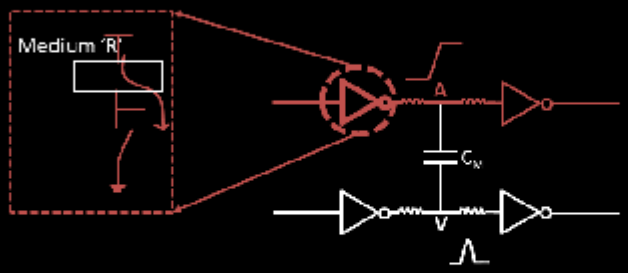
So, one way to reduce glitch, is to reduce the drive strength of aggressor inverter. There are few more advantages of doing this. These transistors are smaller in size, so low overall chip area, thus packing more devices onto the same area.

What about victim? It's exactly reverse. The inverter needs to be strong to retain the logic level on victim net and reduce glitch.

Factors affecting the glitch height

- Aggressor Drive Strength

Stronger the driver, faster the slew, larger the glitch height



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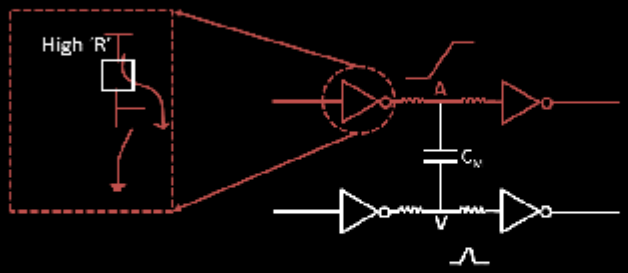
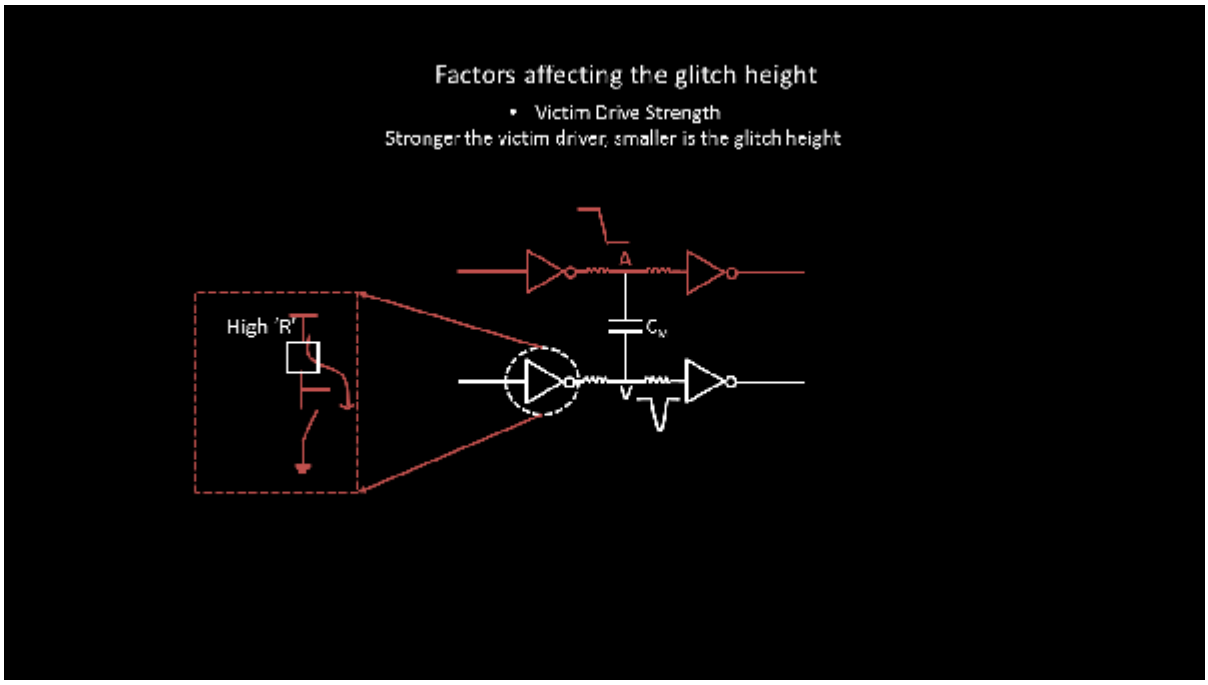
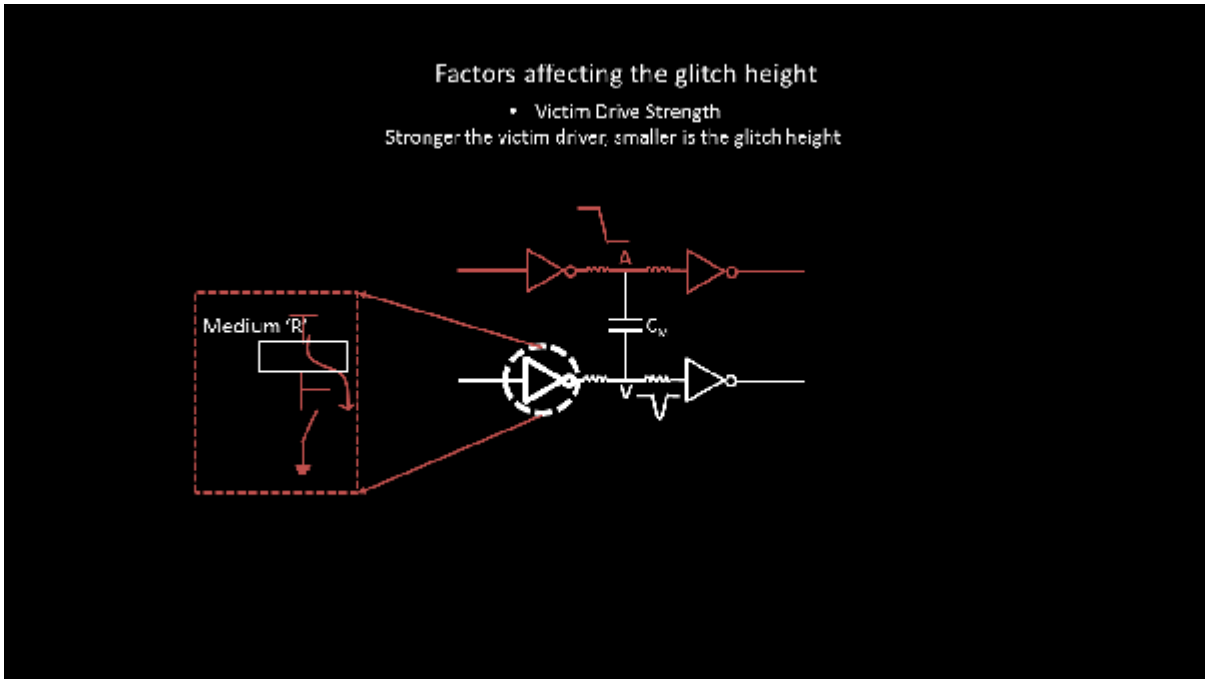
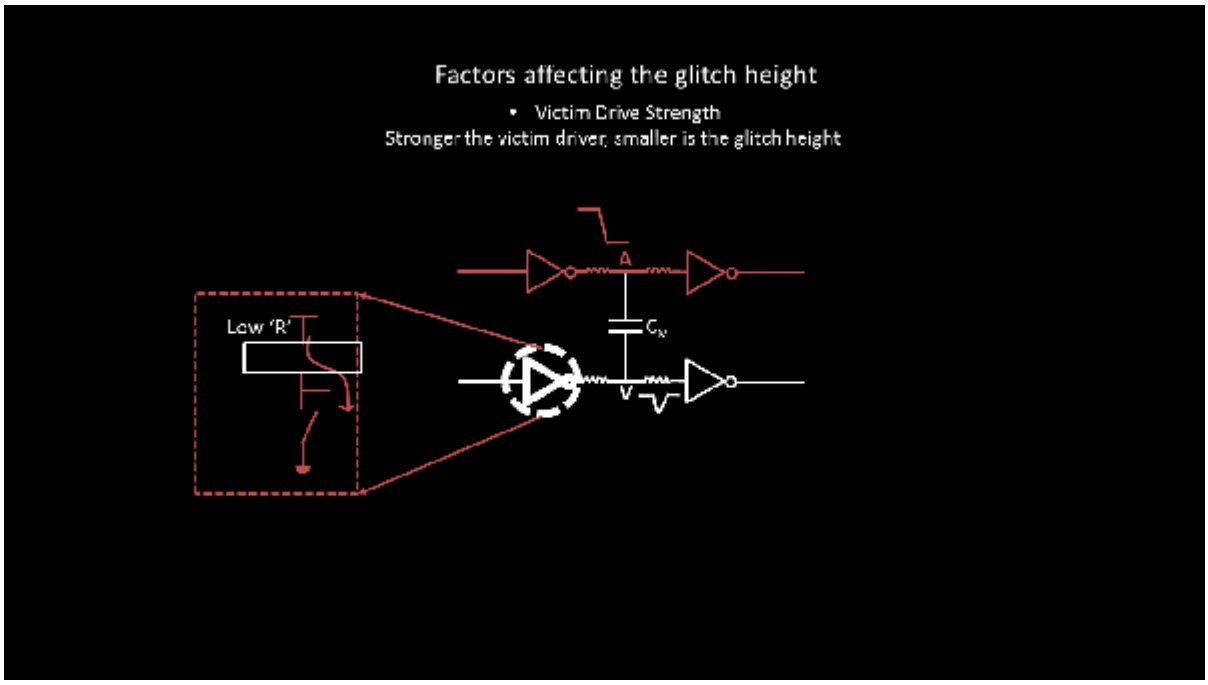
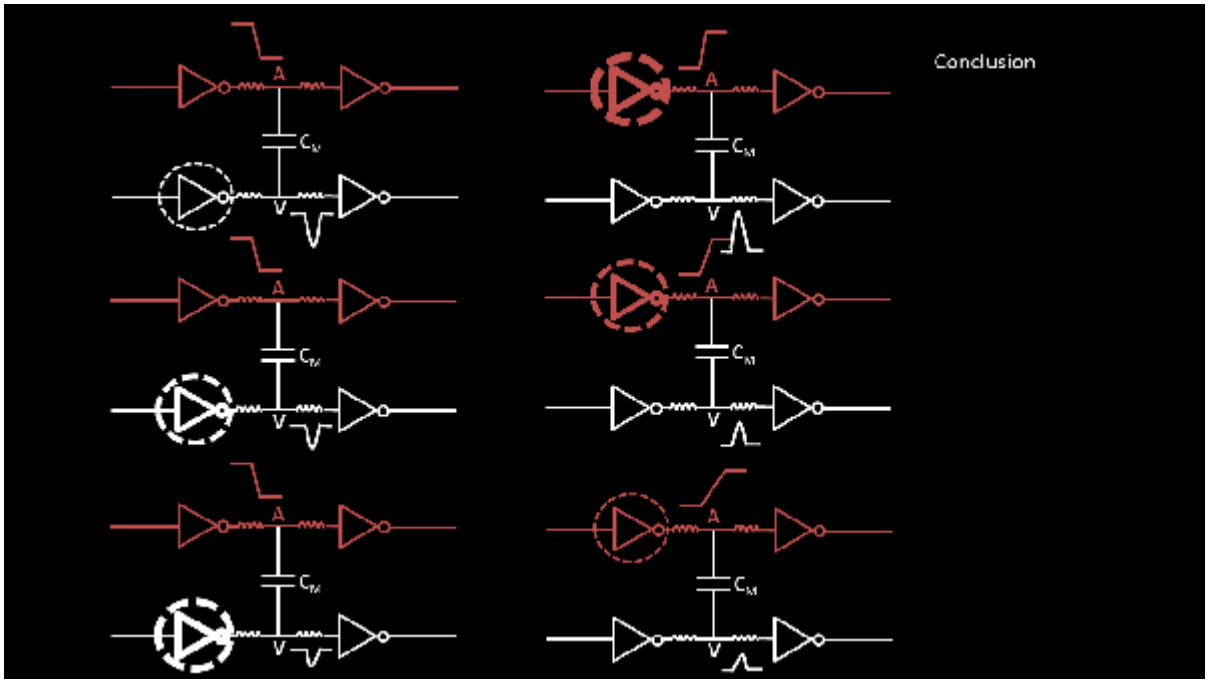






So, looks like, we are back to square one. We save area in the aggressor side, while increase area on the victim side … Grrrhhhhh…. What to do? Let's build a conclusion here in below image





You need to optimize/adjust the inverter sizes in such a fashion, that the area will be optimum and effect of glitch in minimum. I gave a readymade image above, which can be directly used in your real designs to find the optimum size of inverter to reduce glitch, while maintaining optimum area. **We can't eliminate glitch, but always can reduce it and avoid it by some smart techniques, like one shown above.** There are great deal of techniques you can use to reduce glitch, and that makes the *Signal Integrity and Crosstalk* a really vast area of research.