Regular buffer v/s Clock buffer

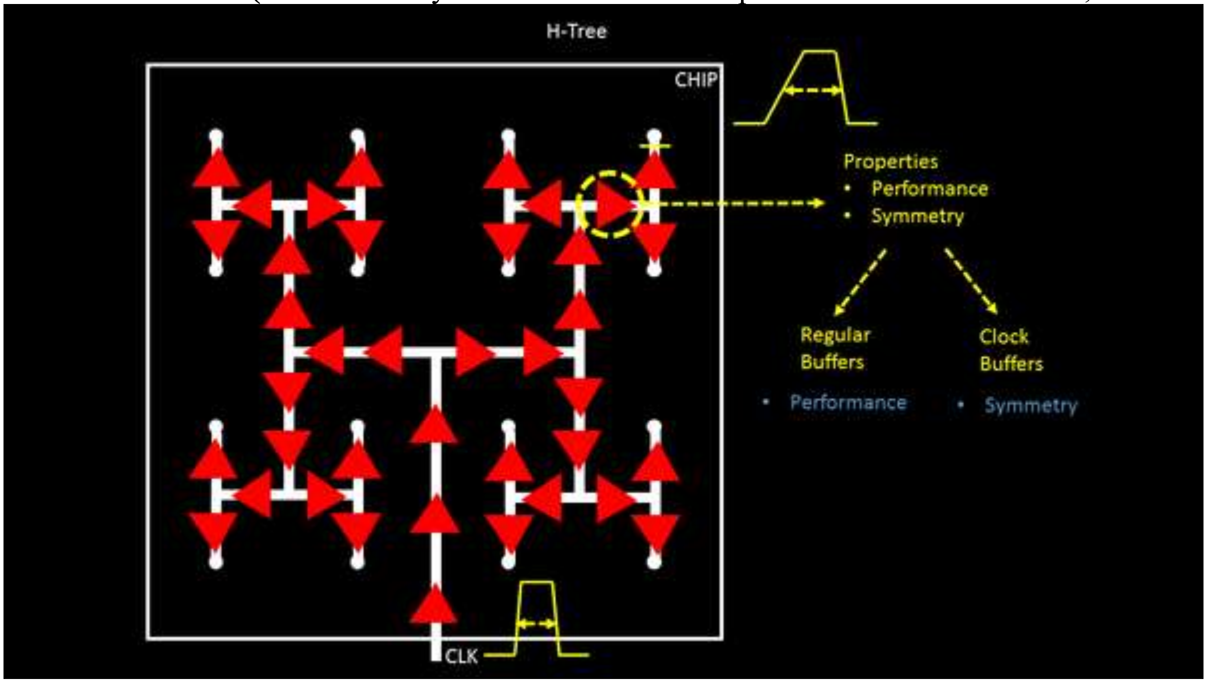
Kunal Ghosh

Everyone, who’s been a part of physical design or STA, must have definitely gone through this. When I thought about it, like 5 years back, as a fresher, I really wished, somebody could had explained me this one in a much

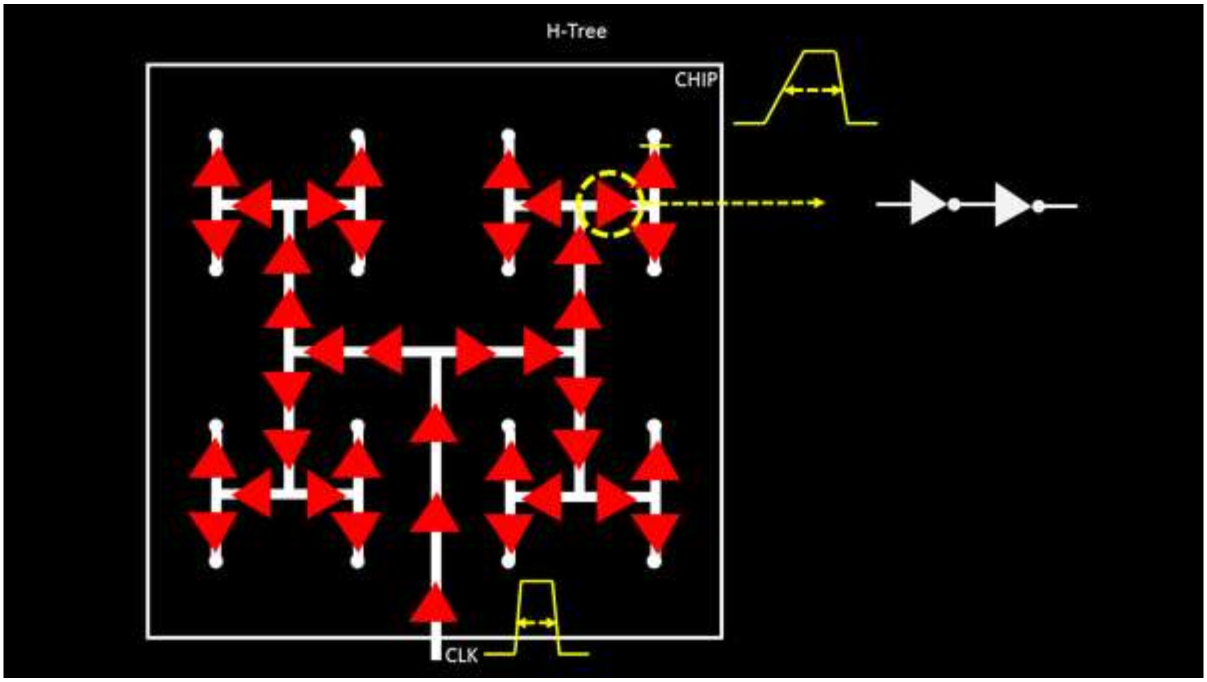
better way, with images. I believe “A picture is worth a thousand words”

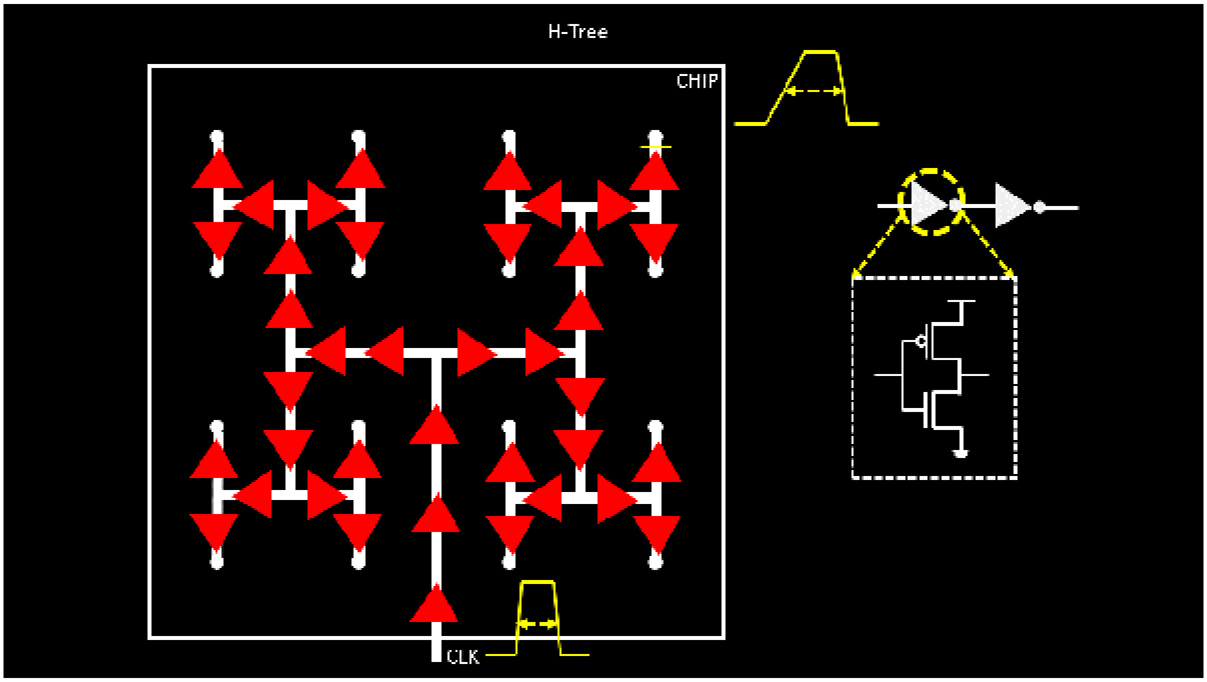
Never mind, I understood the topic and created few images on my own. It becomes relatively simple to understand it this way.

So, the problem is the **asymmetrical waveform**, that you can get at clock endpoint, as shown below. We really (most of the time) don’t want to see these wave-forms in clock network, as it’s the most critical section of the entire circuit. (don’t worry about the complicated circuit below, it’s a clock tree)



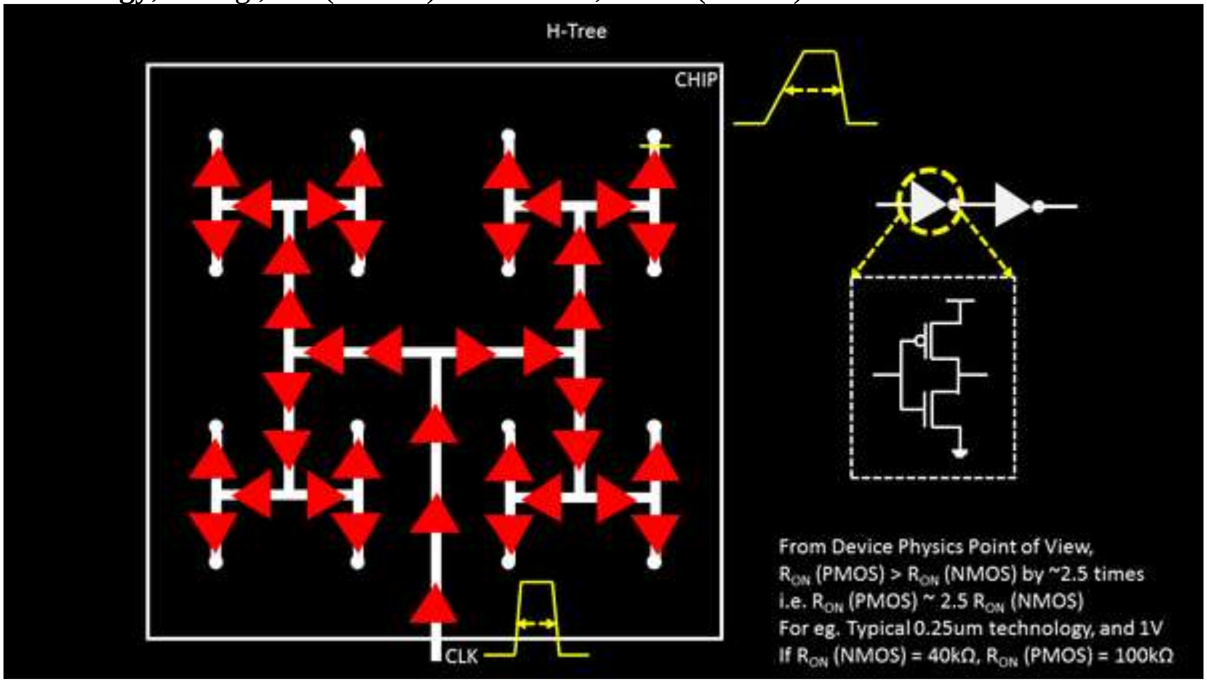
Let’s try to consider this one from **NMOS/PMOS resistance point-of-view**, like below





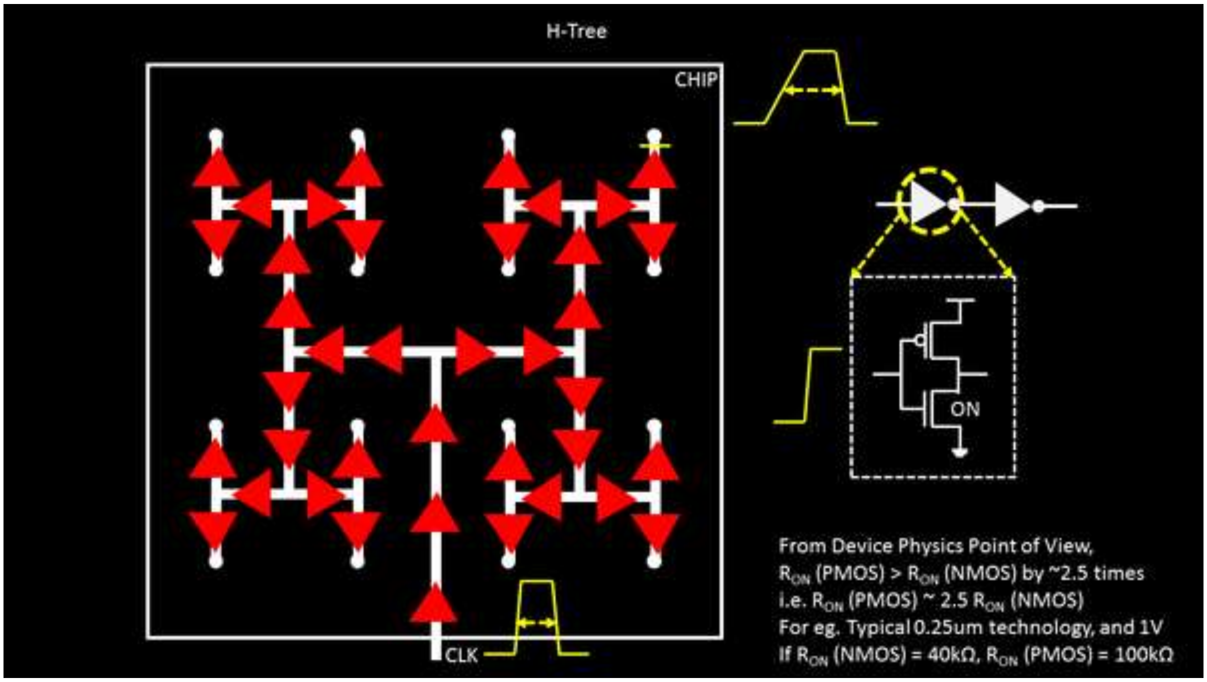
If we look resistance from device physics sense, the resistance of PMOS transistor is typically 2.5 times of an exact size NMOS transistor.

I will prove this from SPICE simulations and some concepts, later, in my video lectures. So, for **0.25-micron technology**, for e.g., if R(NMOS) = 40 k-ohm, then R(PMOS) ~ 100 k-ohm.



From Device Physics Point of View,
R_{ON} (PMOS) > R_{ON} (NMOS) by ~2.5 times
i.e. R_{ON} (PMOS) ~ 2.5 R_{ON} (NMOS)
For eg. Typical 0.25um technology, and 1V
If R_{ON} (NMOS) = 40kΩ, R_{ON} (PMOS) = 100kΩ

So, if **high-to-low delay is D1**, then …… (sentence continued after below 3 images)



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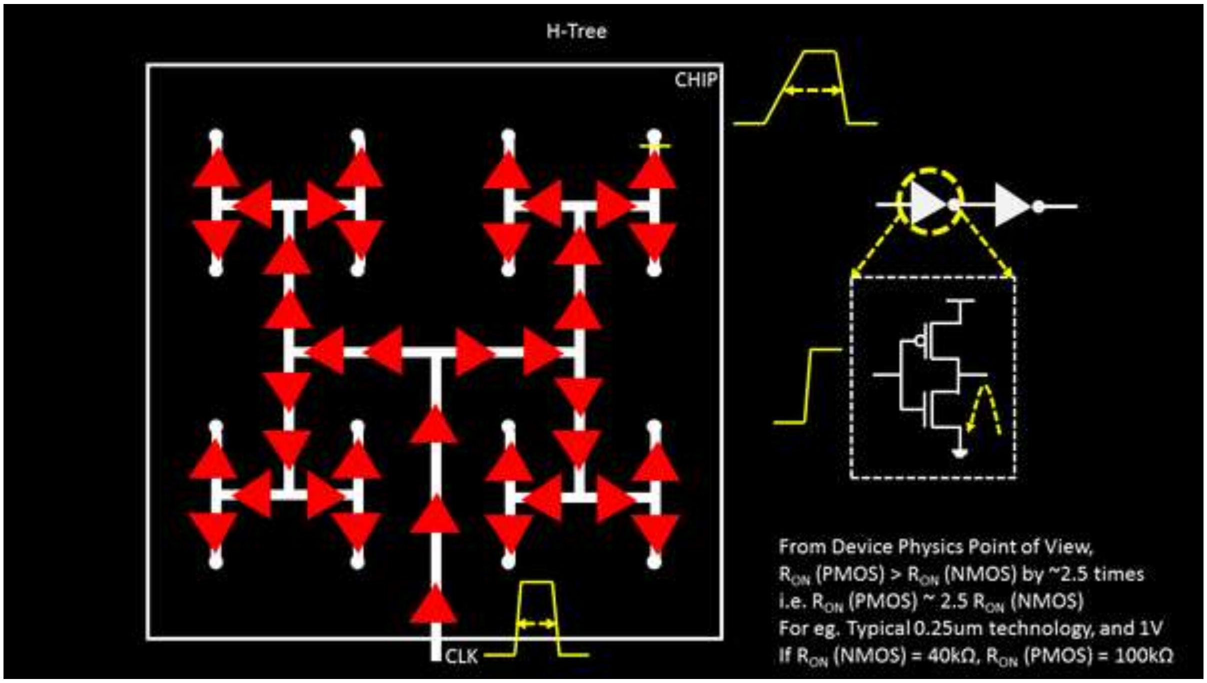

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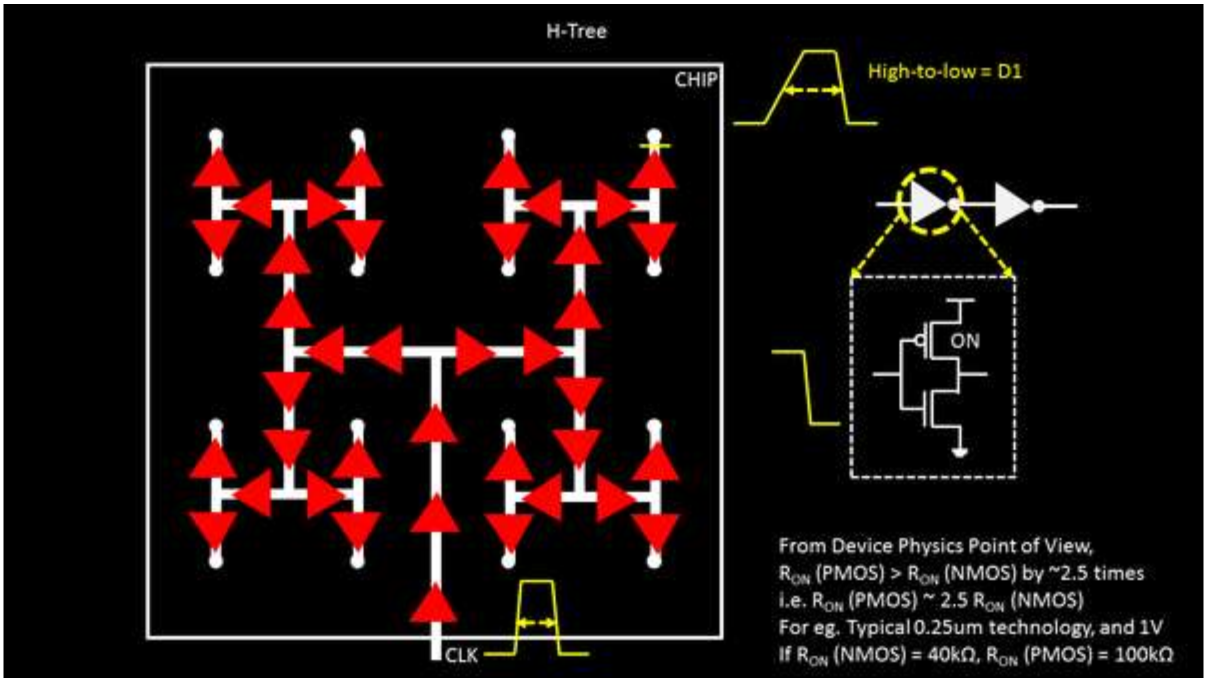
(above sentence continued….) then low-to-high delay is D1+delta, because, same size PMOS (which has a higher resistance than NMOS), takes more time to charge the output load



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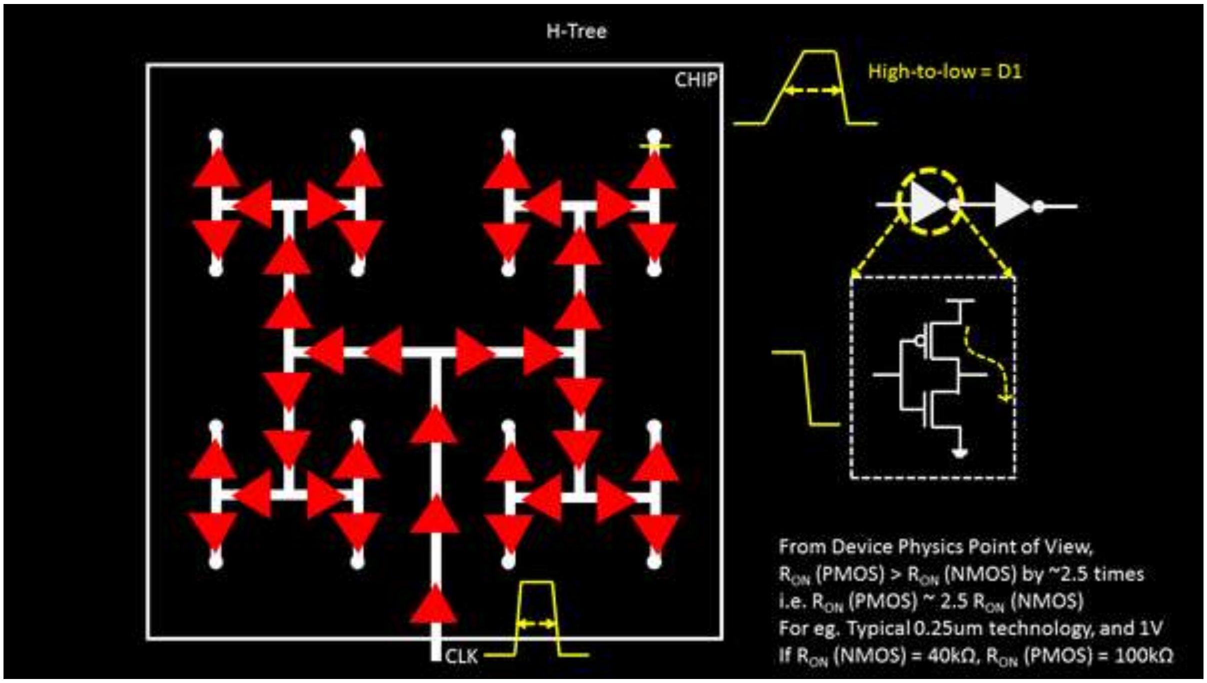

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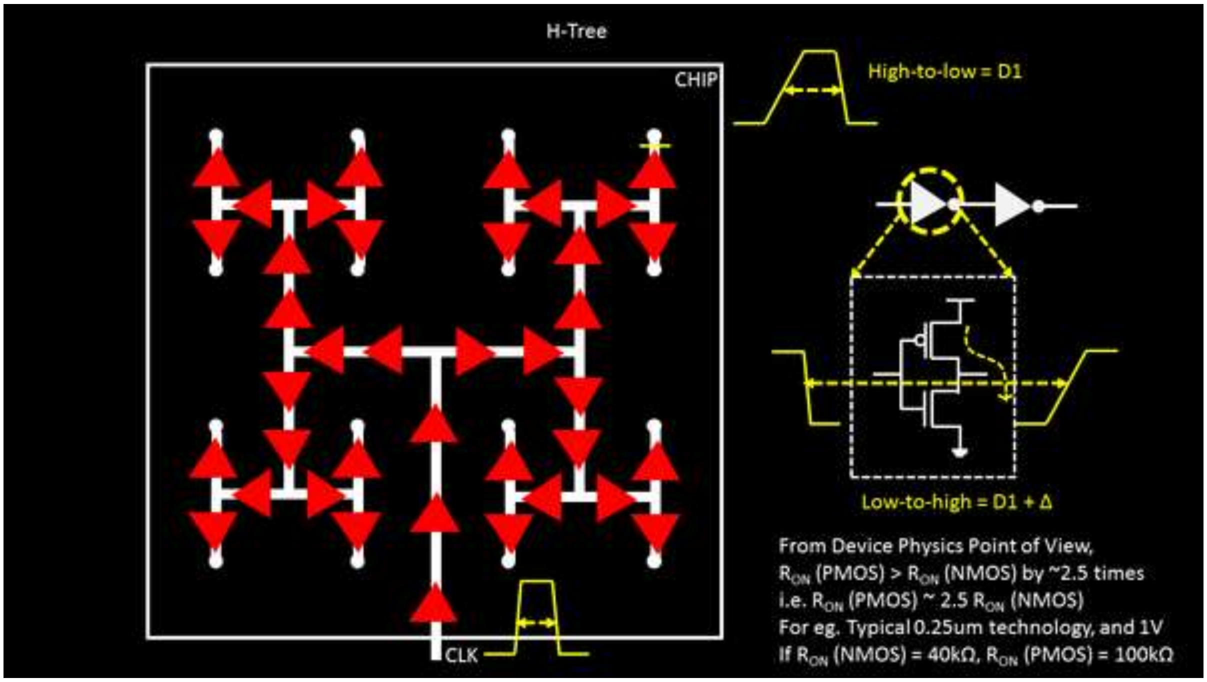

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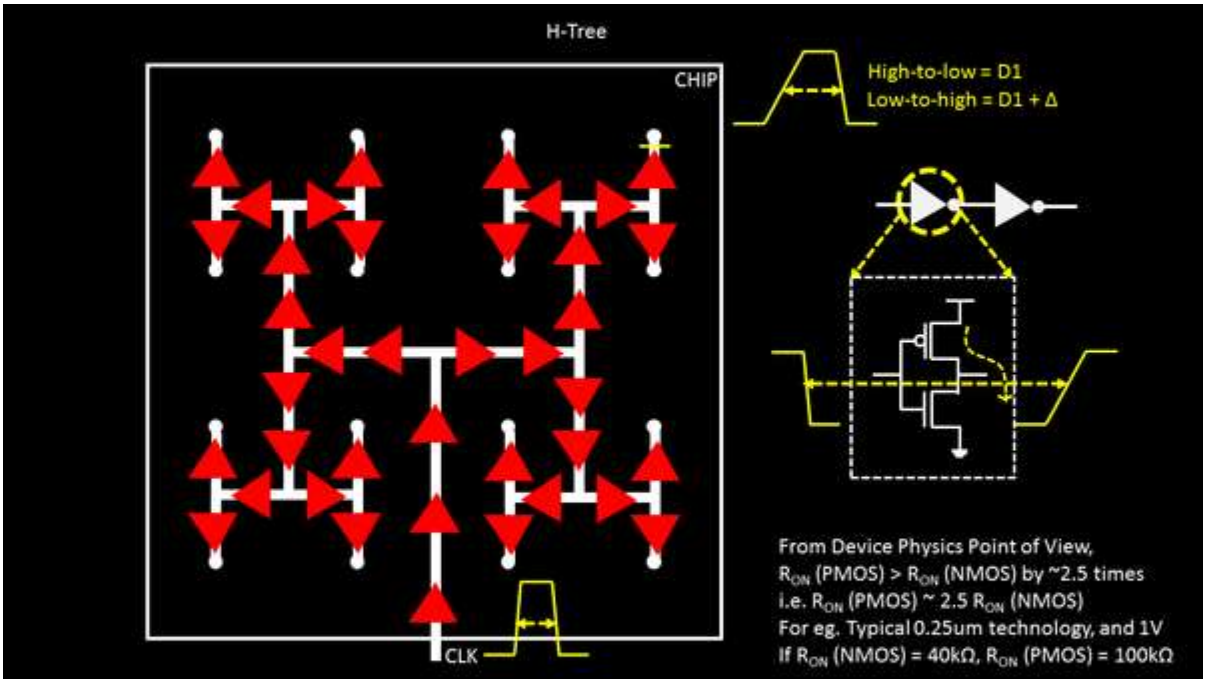
So now, we know the crux of the problem, i.e. **high-to-low delay is not equal to low-to-high delay**



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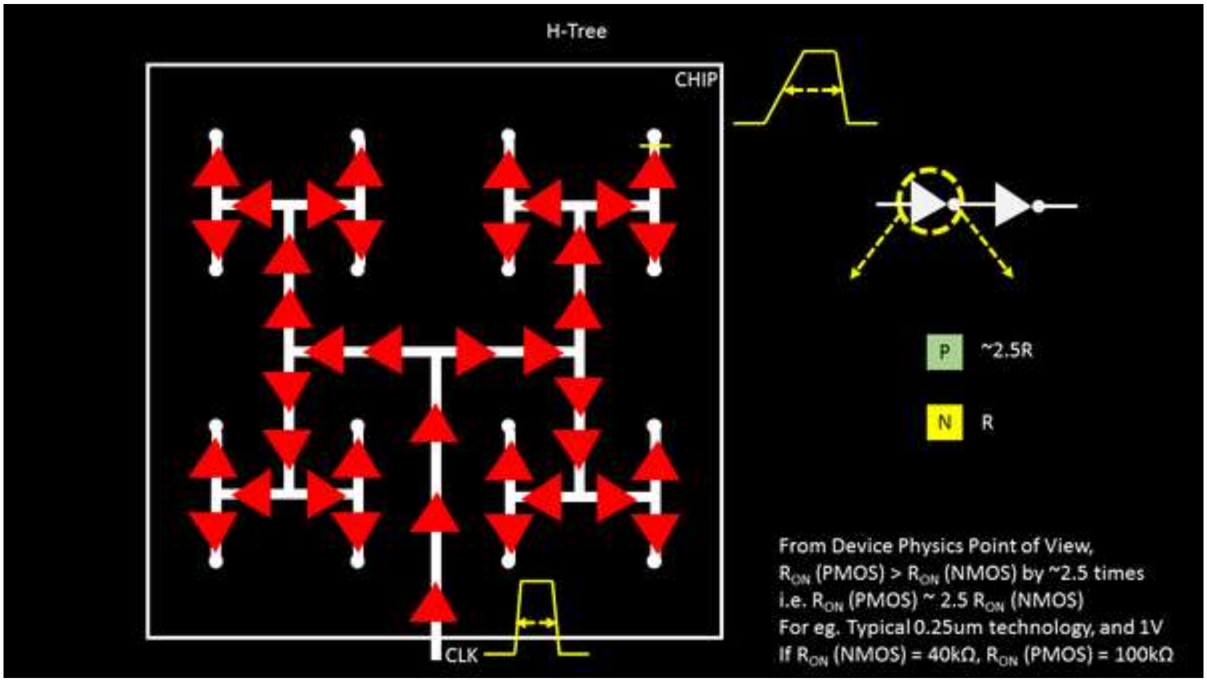
And, so we are seeing that ugly waveform, at the clock endpoint, with un-equal rise-fall times. But, hey, good news, we have a solution to this problem.

We will replace resistance by a hollow box, bigger the box, more items can go through it (low resistance), and vise-versa (high resistance).

NMOS has a resistance ‘R’ and PMOS has higher resistance, ‘2.5R’



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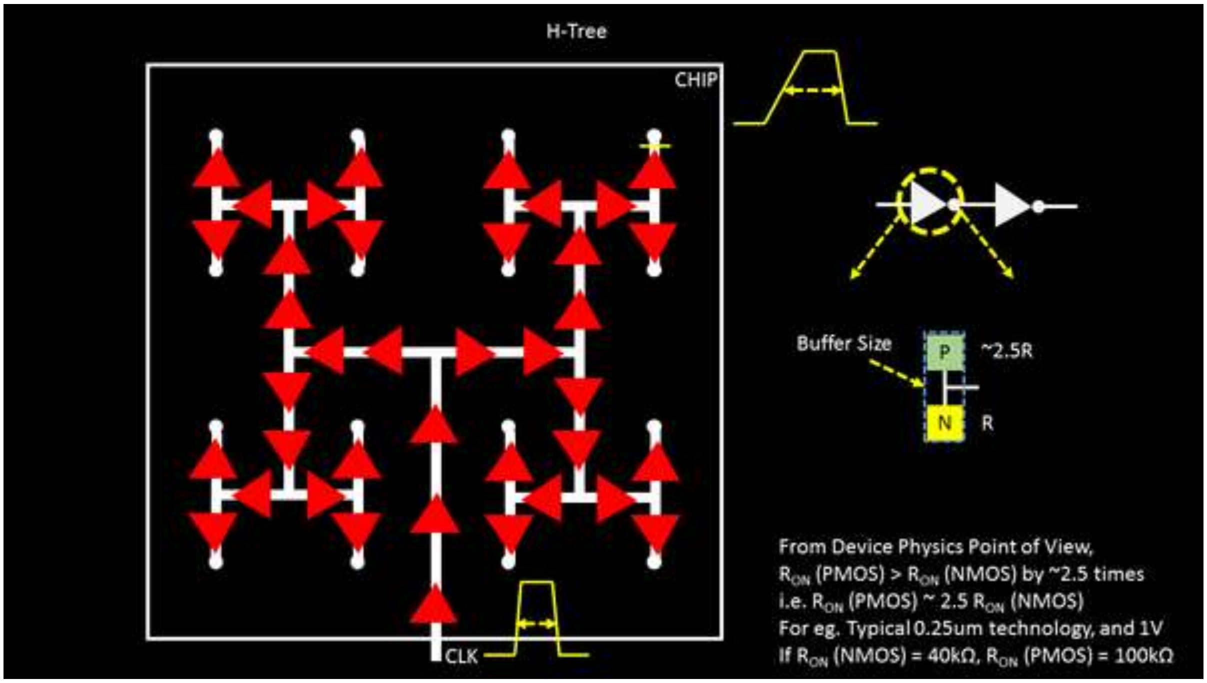
And this will be your buffer (regular) size



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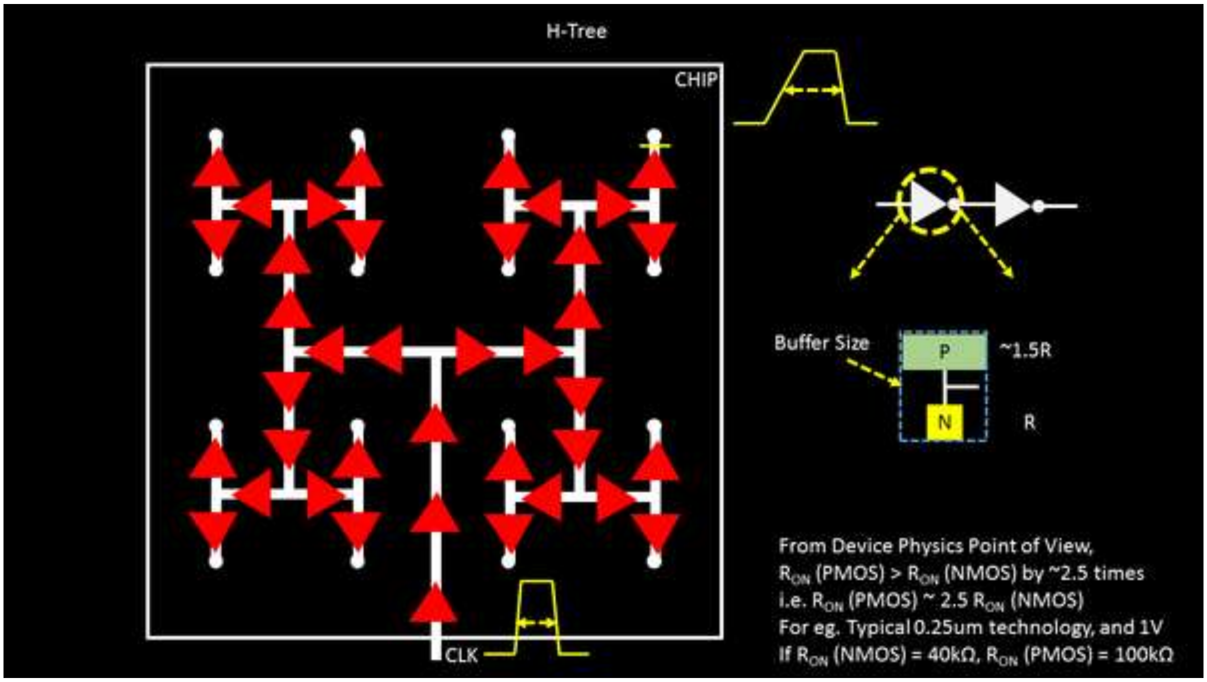
The size looks decent enough, and can be used on non-critical paths, like data-paths. **But definitely can't be used for clock path, due the un-equal rise/fall times, which is due to the difference in resistances.**

Hmmm…

Looks like, we need to fix this resistance to use this one in clock path. Let's use a bigger hollow box for PMOS



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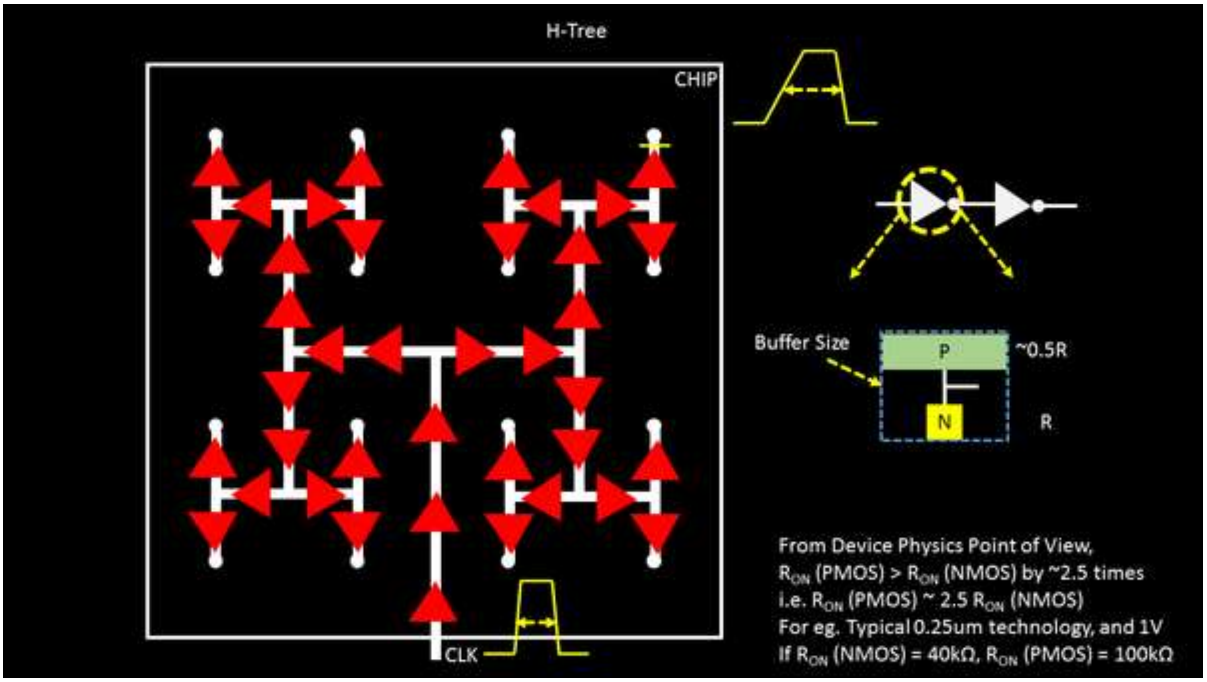
Hey, the resistance just reduced for PMOS, as we increased the width of hollow box. Technically, this 'width' is the channel width (W).

BUT, did you notice, we just increased the size of buffer. Bigger buffer, big chip area, $$$ reduced. Nobody wants to use a smart phone of a size of walkie/talkie.

You know what, its ok to increase the size a little bit, because performance, speed, accuracy are equally important. We will get back on how to smartly build the clock tree

Let'e increase the width even more, such that, the PMOS resistance matches NMOS resistance



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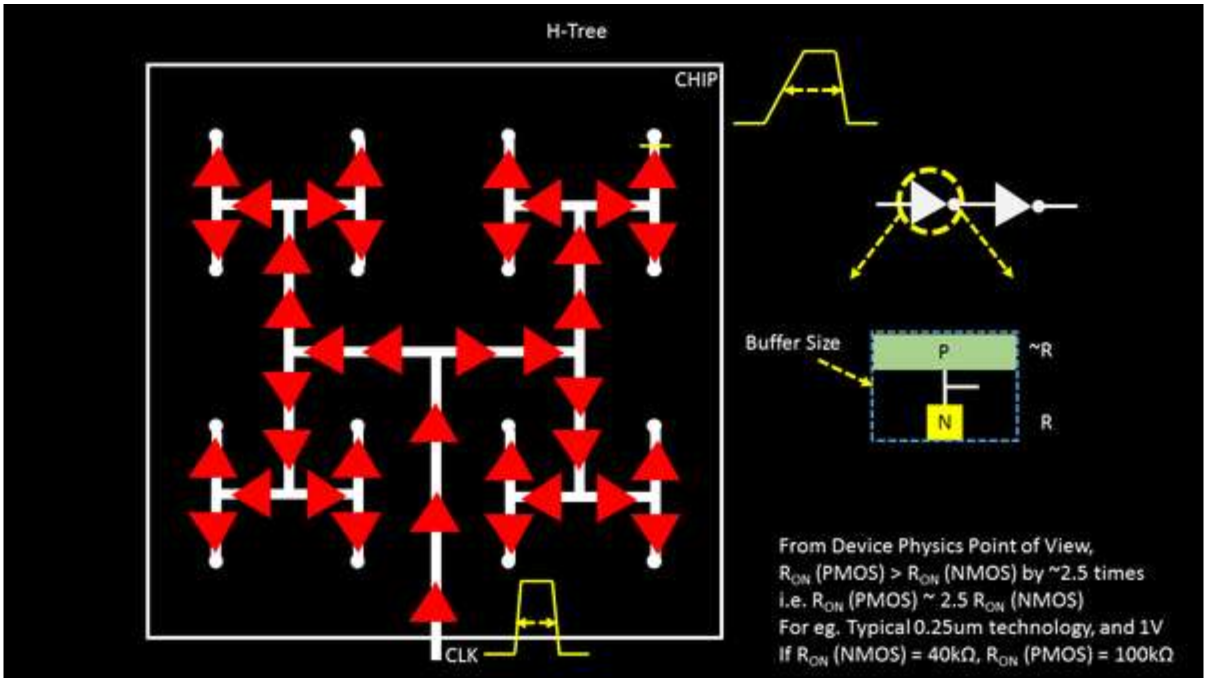
Now, lets observe the **high-to-low delay.**….. (sentence continued after this image)



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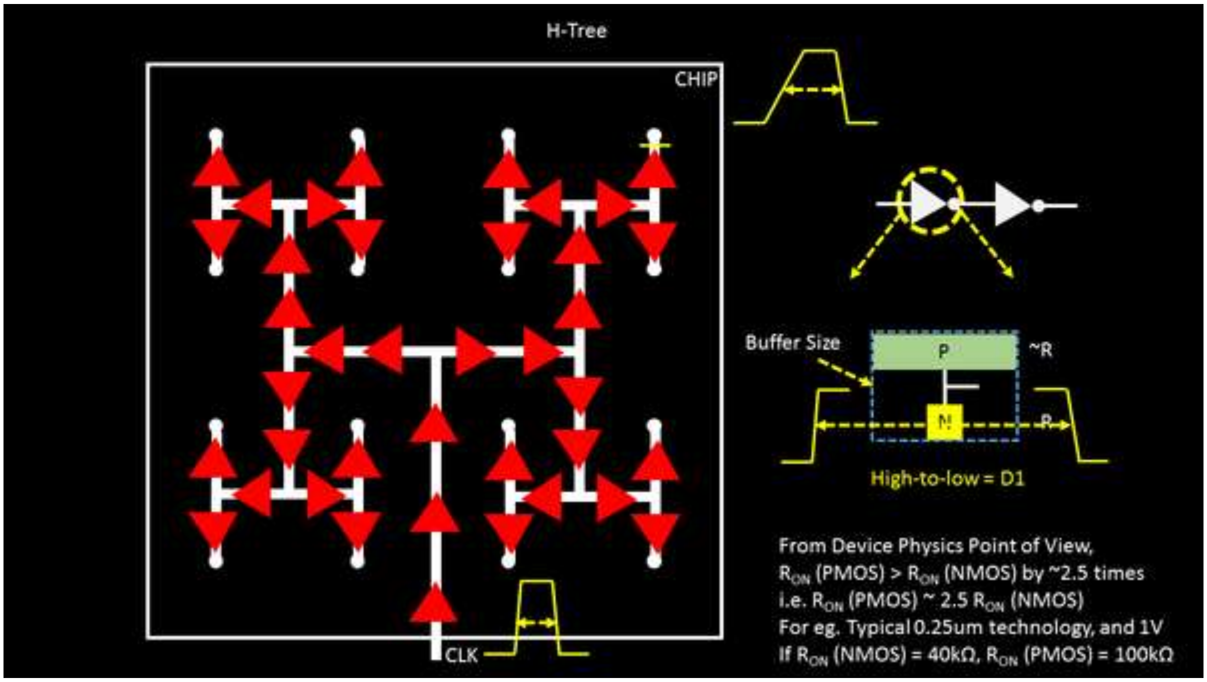
….. (continued from above) and low-to-high delay



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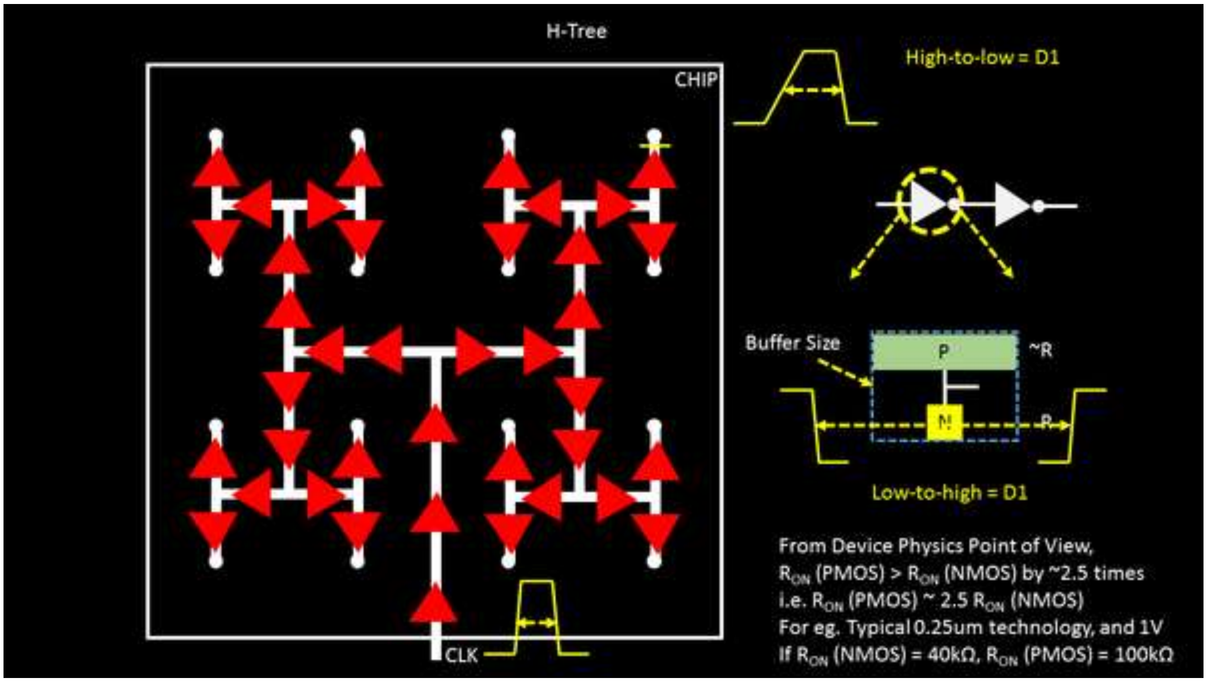
BANG ….. they exactly match. These buffers are specially **designed buffers for clock path**, and are called as **clock buffers**



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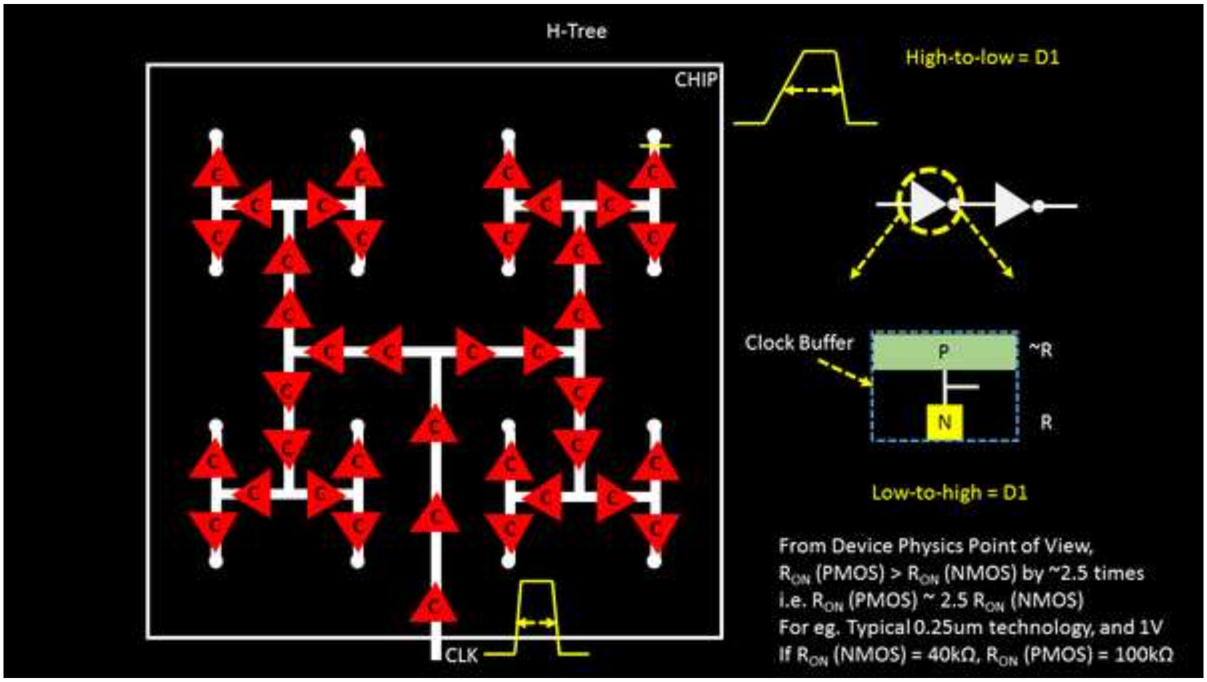
The only price paid using these buffers are

1) **bigger in size, so overall chip area increases**

2) **Very leaky, so should be carefully used, and not heavily**



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Warren Buffet had mentioned in one of his books ***"Price is what you pay. Value is what you get"***

Performance is "Valuable" to customers. You don't want a phone which takes hours to open an app, Do you ?

Luckily, I already had the video as one of the lectures in “*Clock Tree Synthesis*” course on Udemy. Below is the full video on the same.

https://youtu.be/ouSzhV30f1U