I am hidden, but I exist

## Dynamic power dissipation in CMOS

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Meet me, I am "hidden power"

DYNAMIC POWER DISSIPATION IN CMOS

When we are asked about dynamic power dissipation, below 2 things just appear at the top of our mind:

Switching power dissipation

The word 'switching' over here means a lot. It's not just that **inputs are switching**, it's the **outputs also**. Now why do I stress on the word **'outputs also'?** That's because, there's also power dissipation that happens while inputs switch and outputs do not switch. Stay with me, I will introduce it just after this section. Coming back to switching power dissipation, take the below example:
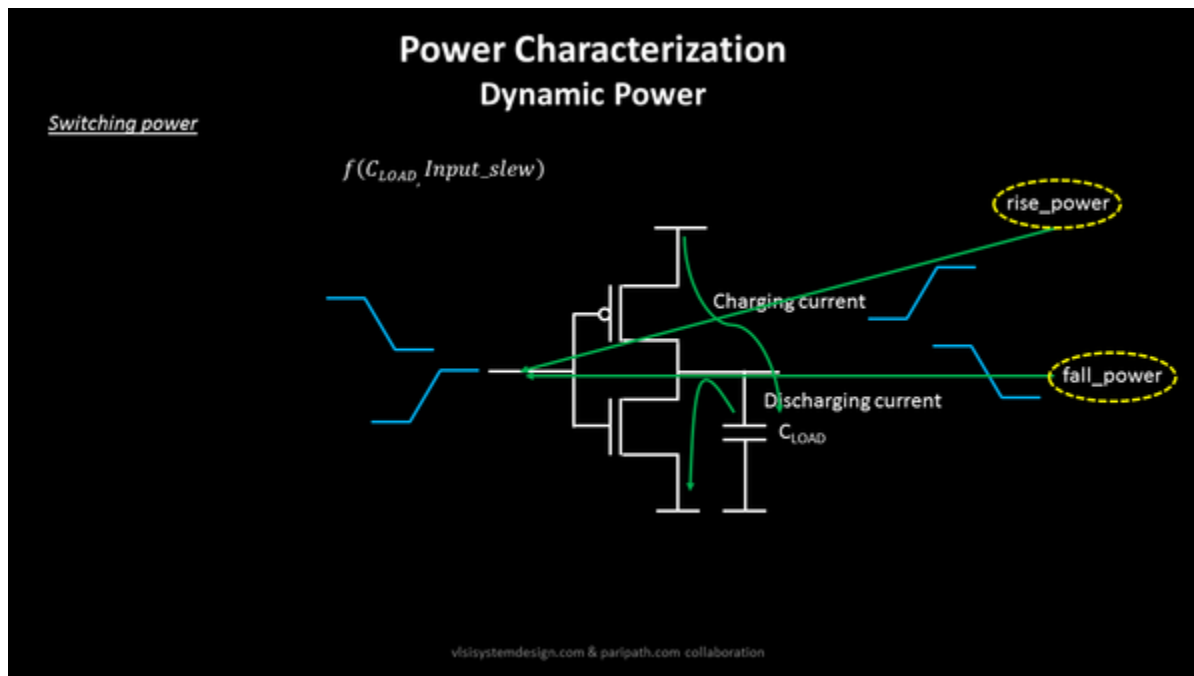

So here, whenever your input switches from logic 1 to logic 0, the output switches from logic 0 to logic 1 and you see charging current flowing from Vdd to C_{LOAD} which results to rise_power (this is a liberty attribute used to denote rise_power). And vice-versa holds true when input switches from logic 1 to logic 0

This was easy…Next, there is another kind of power that dissipates when your inputs and outputs are switching, that's short-circuit power

Short circuit power dissipation in CMOS inverter

**This power dissipation is another beast**. Look at below image:
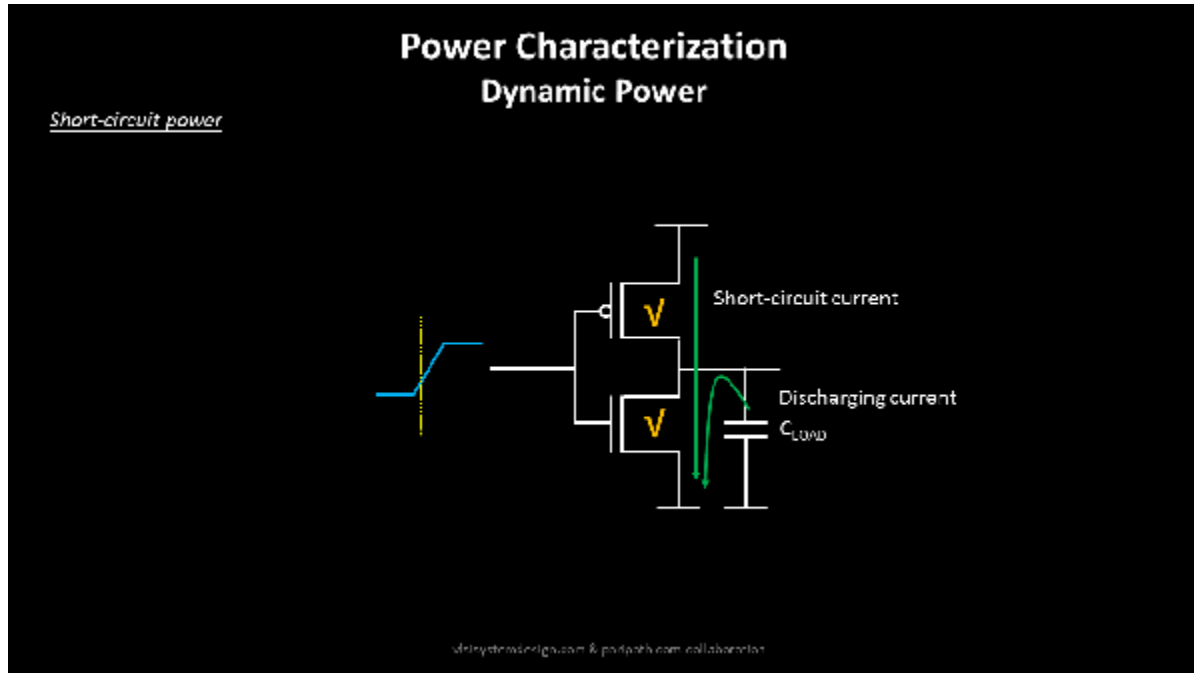
When your input is at logic '0' and assuming your VDD is at 1.8V (considering it's a **180nm technology node**), why do you think, from physics point of view, does your PMOS turns ON? The reason is, logic '0' at gate means its at 0V, Vdd is at 1.8V, the PMOS Vgs = 0 – 1.8 = -1.8v which is far above the threshold voltage of PMOS transistor, which makes the PMOS to turn ON

Similarly, Vgs of NMOS is 0V – 0V = 0V, which is below the threshold voltage of NMOS transistor and hence NMOS is OFF. Now look at the highlighted area in the input transitioning waveform. In that area, if gate input rises from 0v to (say) 0.5v, the Vgs of NMOS is 0.5v, which is just above the threshold voltage of NMOS (assuming NMOS Vt is 0.2V for 180nm technology node), so it just turns ON

Now the Vgs of PMOS is roughly, say 0.5v – 1.8v = -1.3V which is again, far above threshold voltage of PMOS transistor, so your PMOS transistor is still ON. You see, at this point, both PMOS and NMOS transistor are ON. Looking Vdd at higher potential, and GND at lower potential, there is now a direct path from Vdd to Gnd.

That's short circuit current, and hence the name short-circuits power dissipation

So now the big question? **What if the outputs do not switch, while only the inputs switch, like the below case of AND gate**
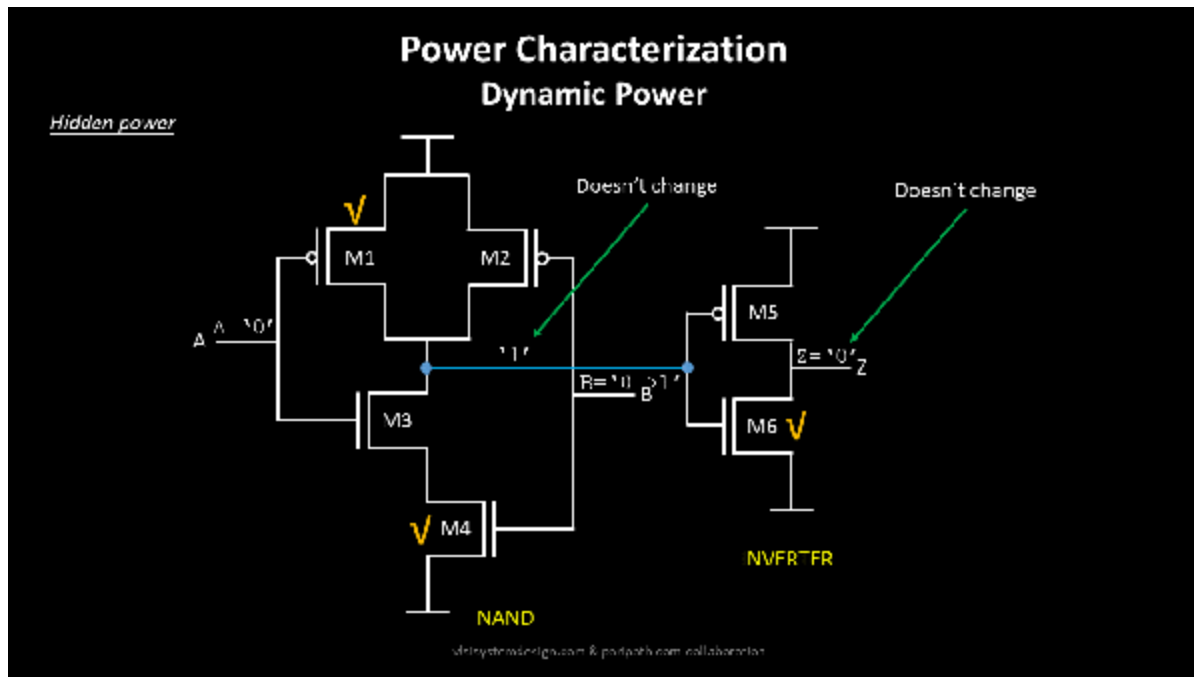
Here, if you see, even though your input 'B' switches from logic '0' to logic '1', your NAND output and hence, the AND output doesn't switch. So do we still see power dissipation in these kind of scenarios?

Hidden power

That's me "hidden power". That's how I introduced myself in the beginning of the post. Now even though, in the above image, the outputs do not switch, the switching of input 'B' creates a unique path for current flow from Vdd to Gnd. Look at below image:
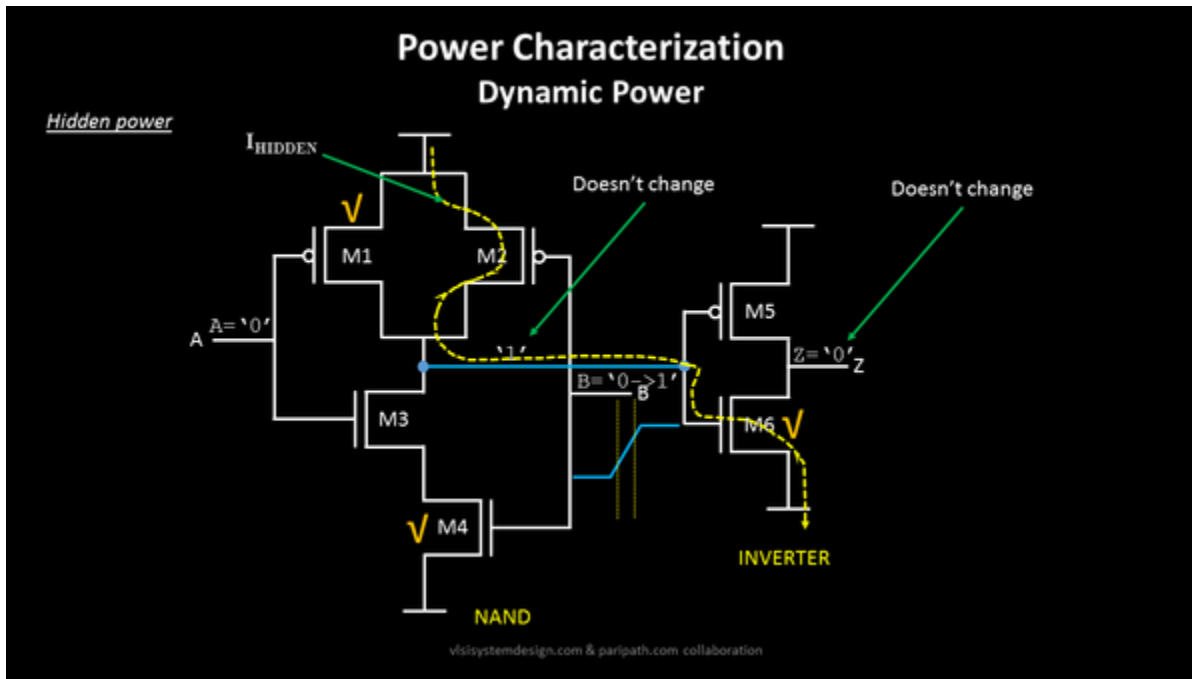
During the transitioning of 'B', due to similar reasons of Vgs being greater than threshold voltage of PMOS and NMOS transistors, M2 is ON momentarily, and I flow from Vdd – M2 – M6 – GND. Since I am hidden inside the boundary of the cell, the name **hidden power**

This brings me to very important point about myself, that if I am hidden, doesn't mean I do not exist…