# Clk-to-q delay

## LIBRARY SETUP AND HOLD TIME

Kunal Ghosh

I have been receiving multiple queries on **what is clk-to-q delay, how's it different from library setup time and library hold time**, etc.

I mentioned in my discussions, that the videos on CMOS digital circuit will be uploaded soon, but looks like, it might take some time, and hence decided to upload few images from my CMOS course, to explain the difference between all of them.

We will learn about it in two parts. This post will explain what is present inside the flipflop i.e. negative and positive latches, and the transistor level implementation of both.

In next post, we will explain, **how a positive edge triggered flip flop is made using positive and negative latches,** and come up with equations and differences between clk-to-q delay, **library setup time and library hold time**

Let's begin with the first image **which shows what's present inside flip flop and introduction to negative latch**

## check out the below series of images.

Hope these set of above images, clearly distinguishes **what's a positive latch, what's a negative latch and what happens when clock is 'low' or 'high'**. I would say glance through the images one more time, so that the concept is clear.

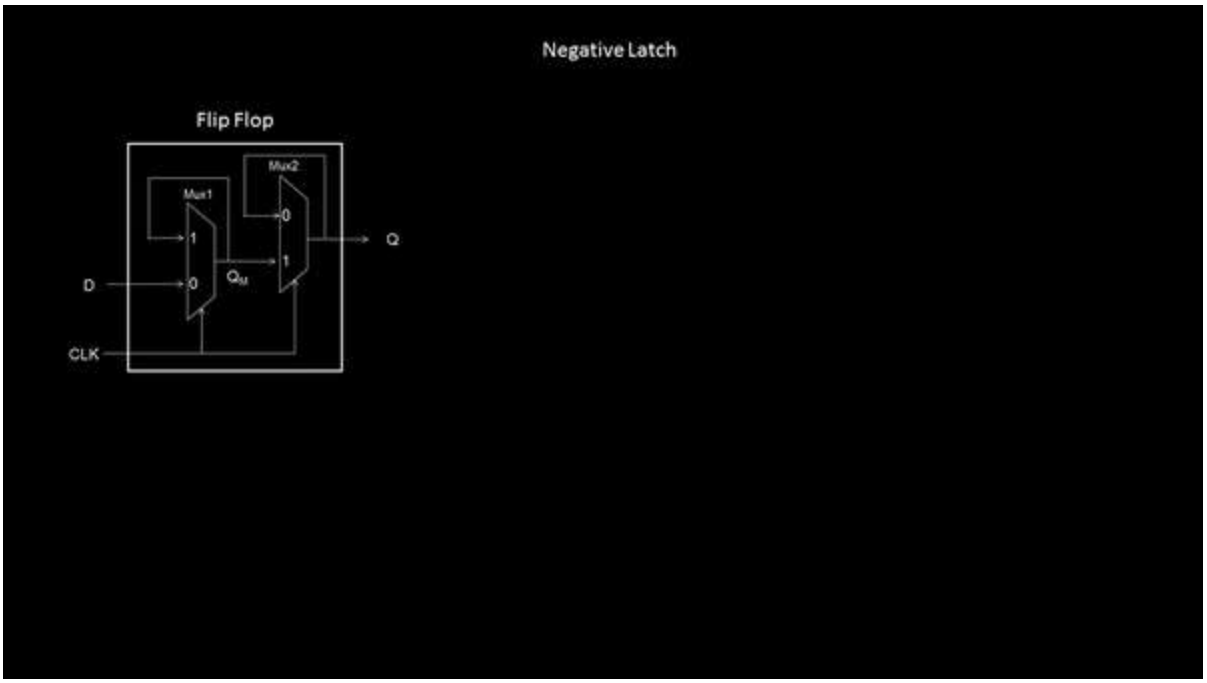
In my next post, I will connect the output of negative latch to input of positive latch, and throw some light on clk-to-q delays and the setup and hold times internal to flip flops

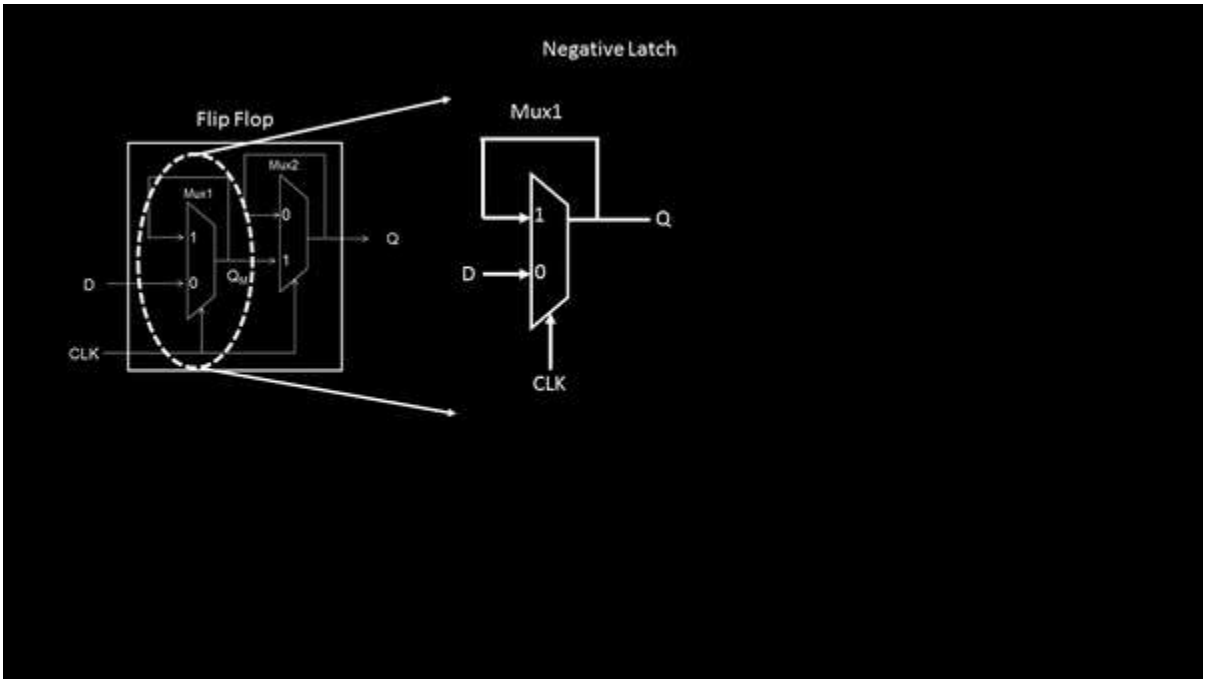
I would also like to request everyone to share their experiences/doubts in this post

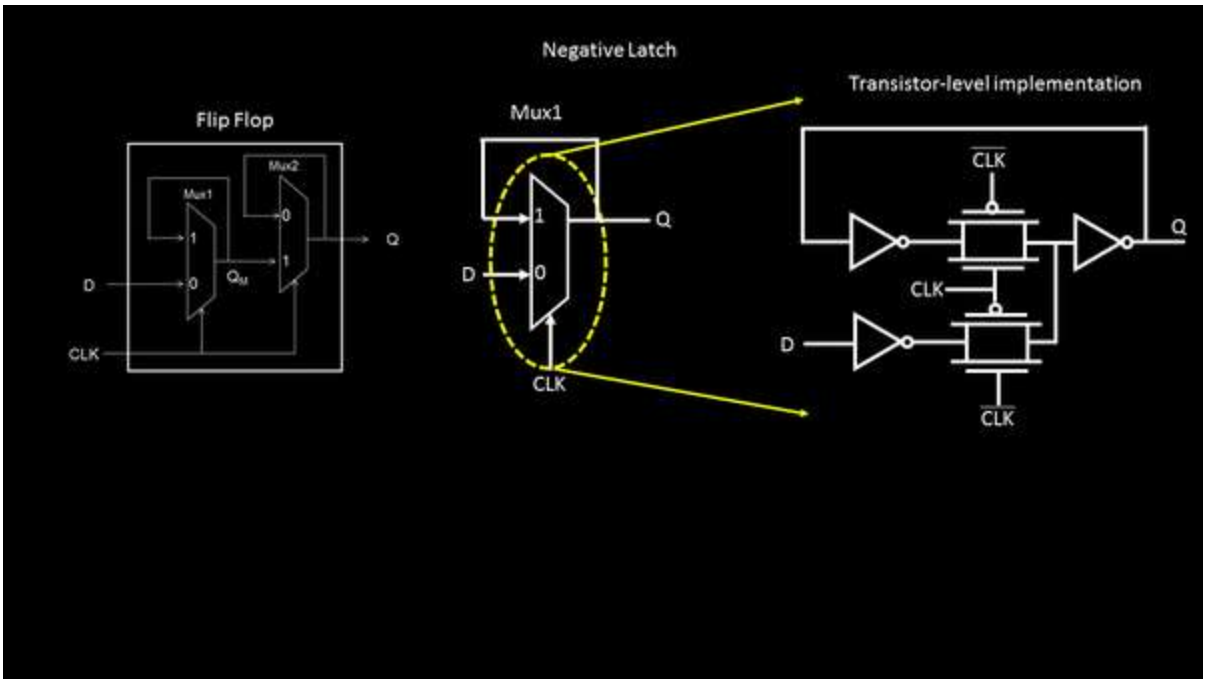
Happy Learning

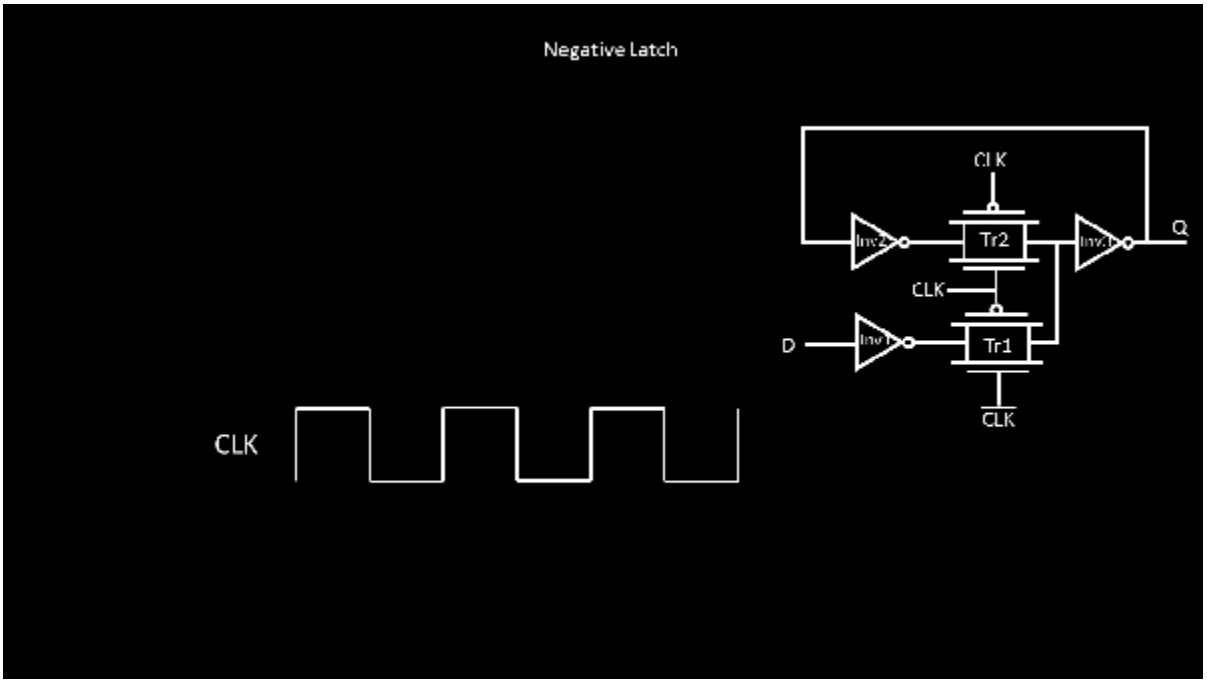
Thanks

VSD Team


Negative Latch
Flip Flop
Mux2
Mux1
0
1
Q
1
D
0
$Q_M$
CLK

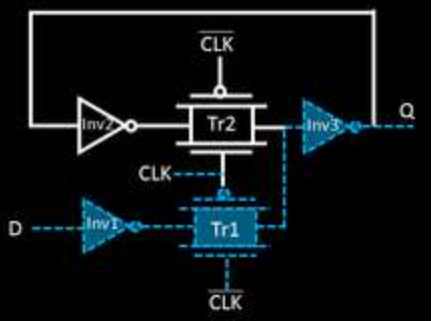

Negative Latch
Flip Flop
Mux2
Mux1
0
1
Q
1
D
0
$Q_M$
CLK
Mux1
1
Q
D
0
CLK


Negative Latch
Flip Flop
Mux1
Mux2
D
CLK
Q
$Q_M$
Mux1
D
CLK
Q
Transistor-level implementation
CLK
CLK
D
Q
CLK


Negative Latch
CLK
Tr2
CLK
D
Tr1
Q
CLK
CLK

## Negative Latch

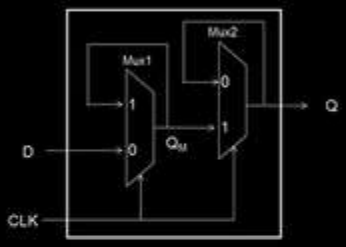
When CLK is 'low', "Tr1" turns ON (i.e. PMOS/NMOS of Tr1 are ON), and input 'D' is latched to output 'Q'

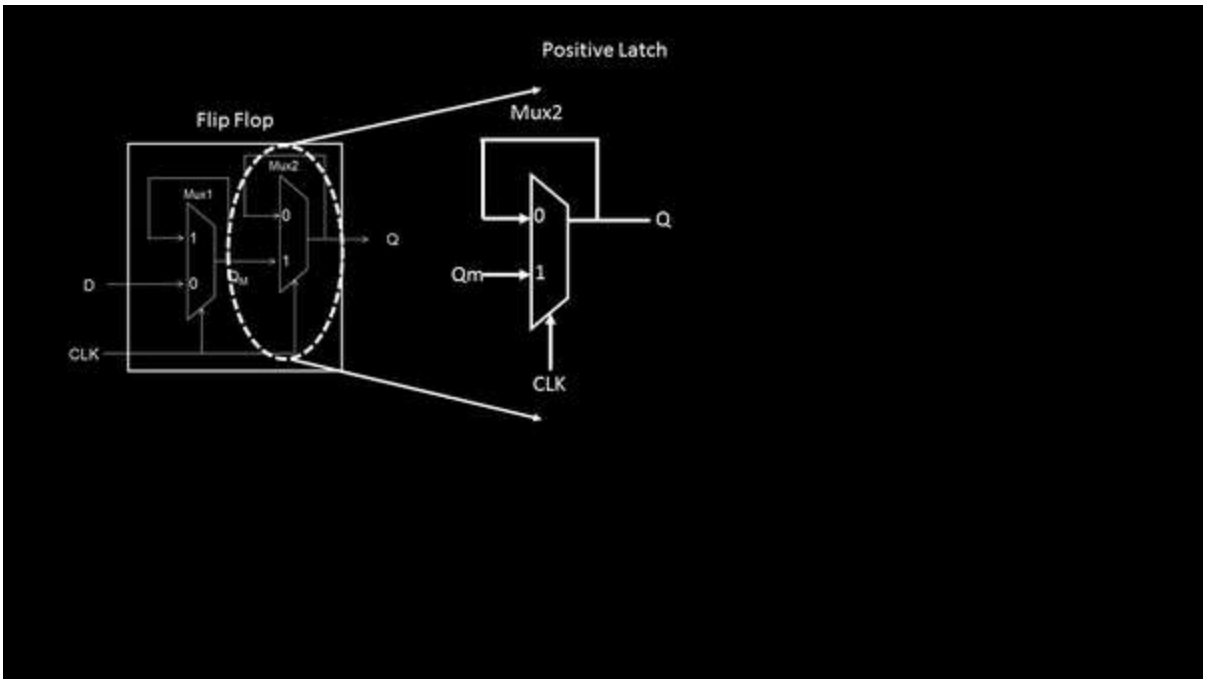


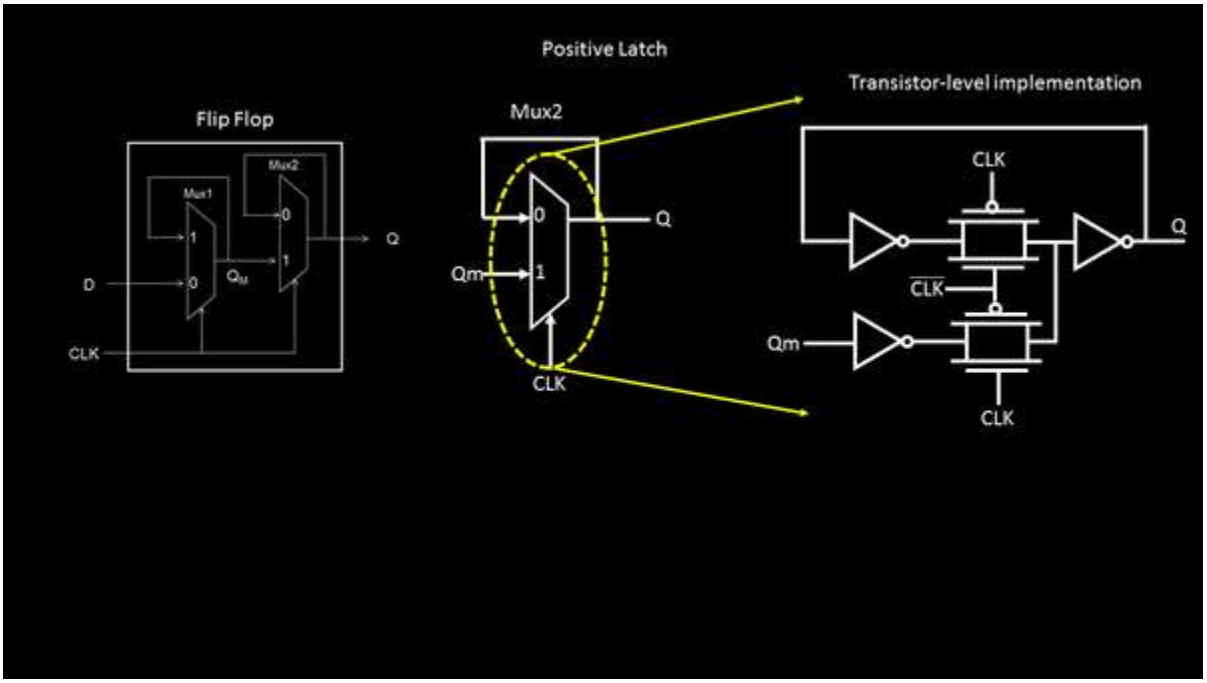


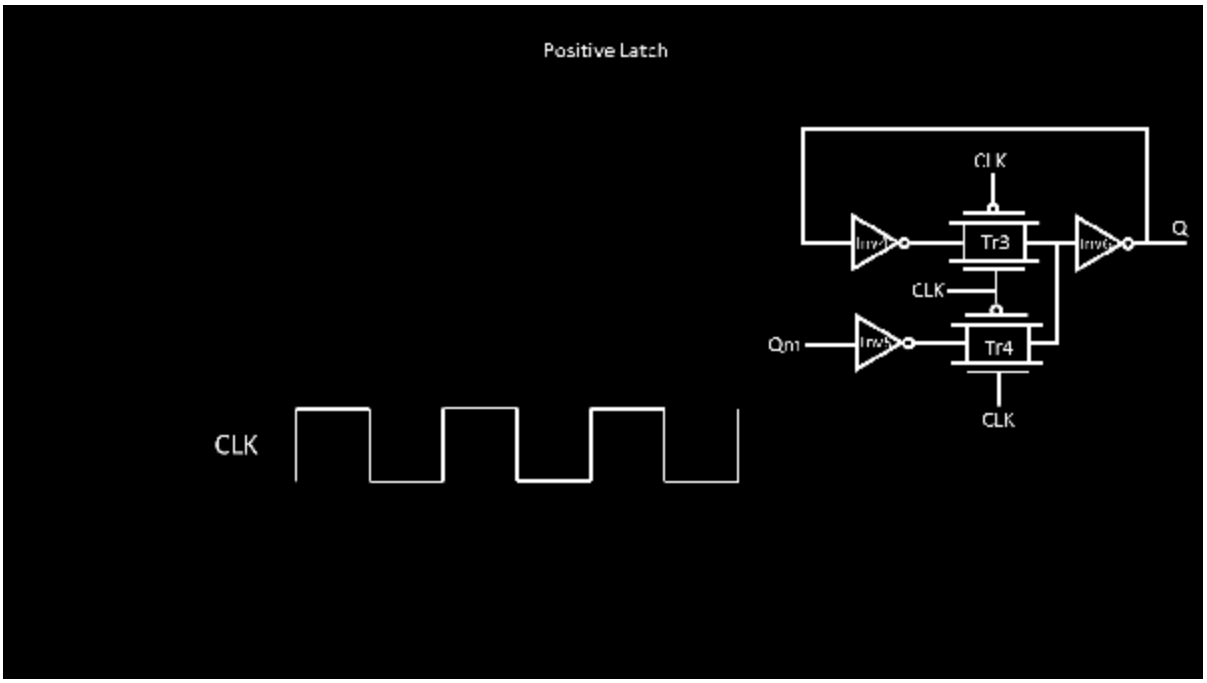
## Positive Latch

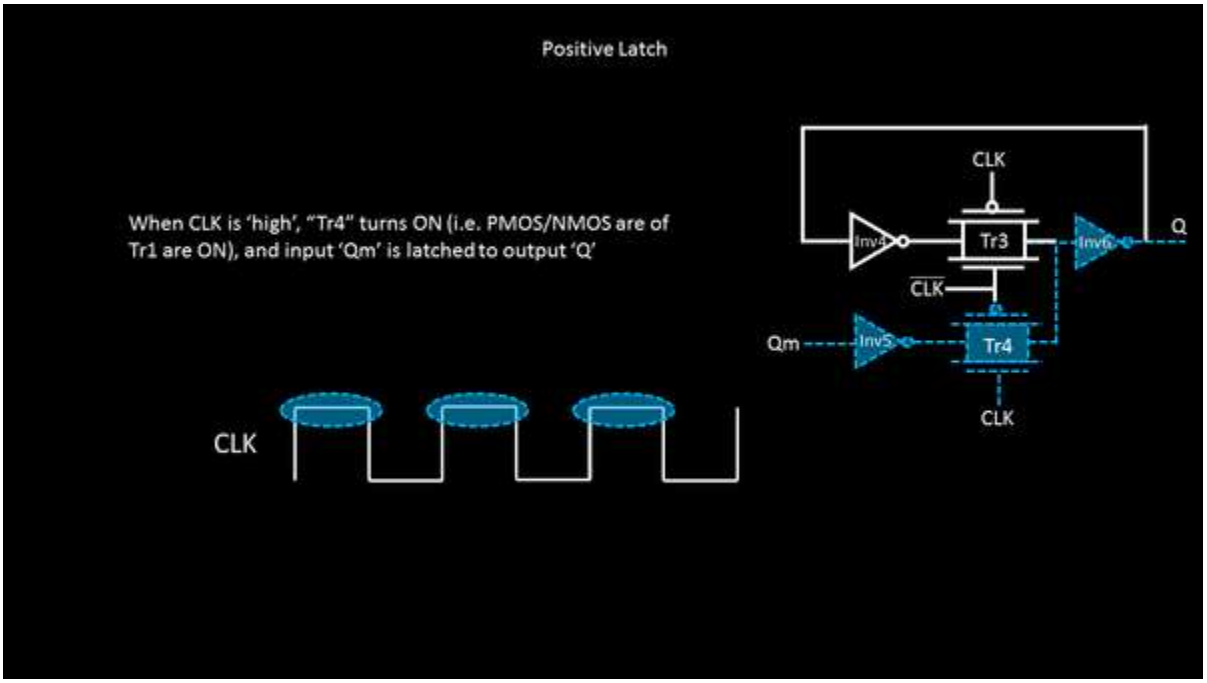
Flip Flop

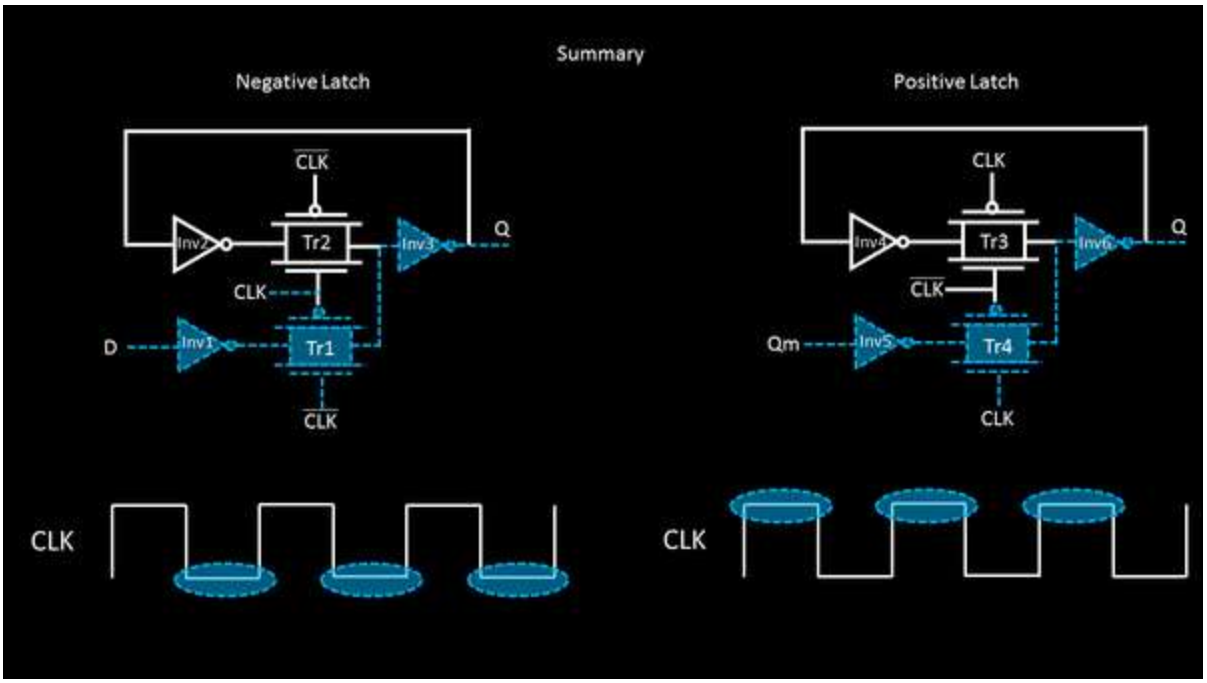


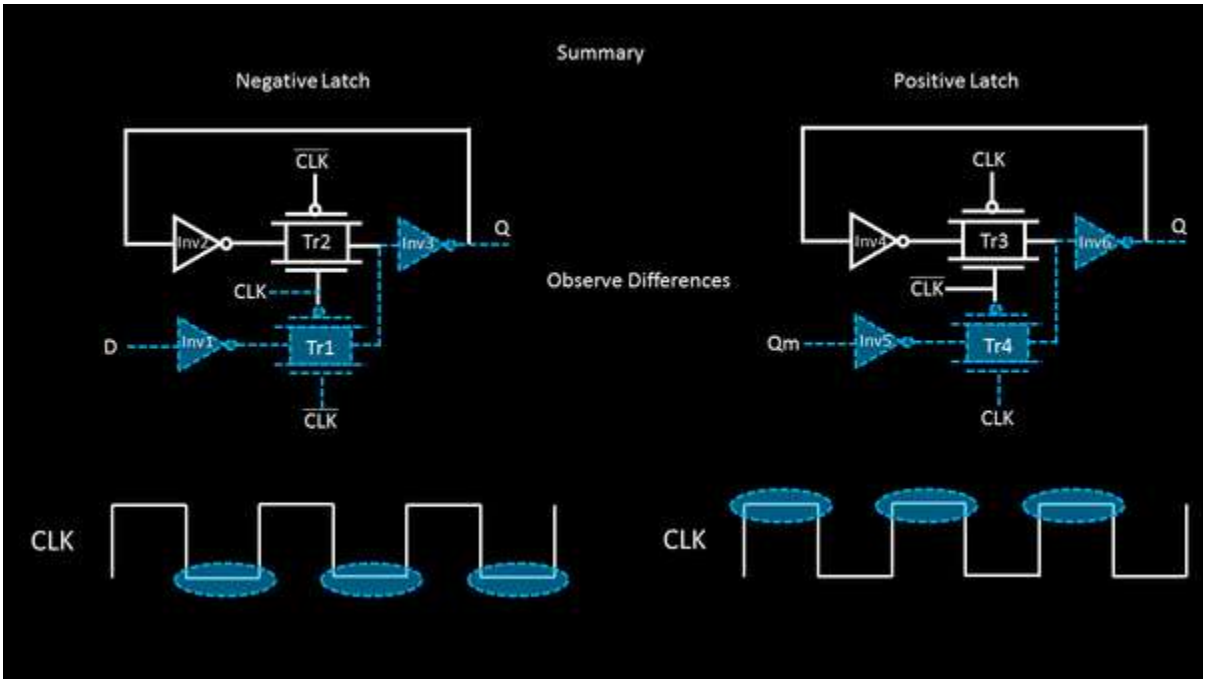

Positive Latch
Flip Flop
Mux2
Mux1
Mux2
0
1
0
1
Q
D
0
$Q_M$
Qm
1
Q
CLK
CLK

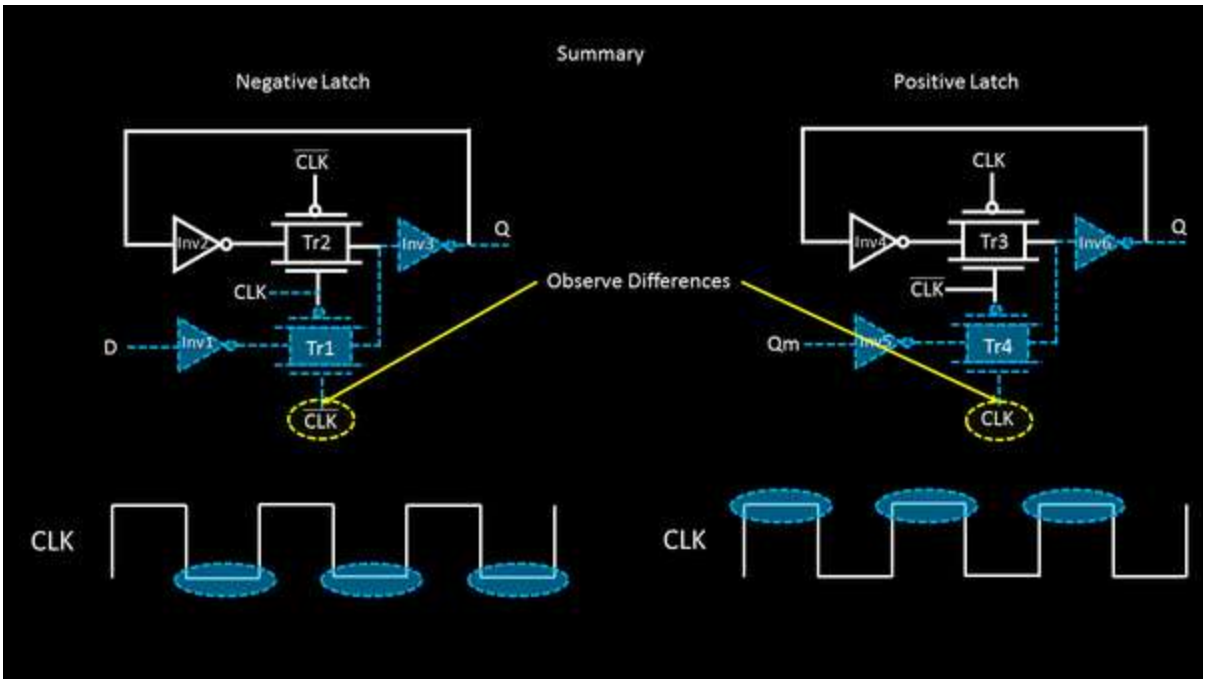

Positive Latch
Transistor-level implementation
Flip Flop
Mux2
Mux1
Mux2
0
1
0
1
Q
D
0
$Q_M$
Qm
1
Q
CLK
CLK
CLK
Q
$\overline{CLK}$
Qm
CLK

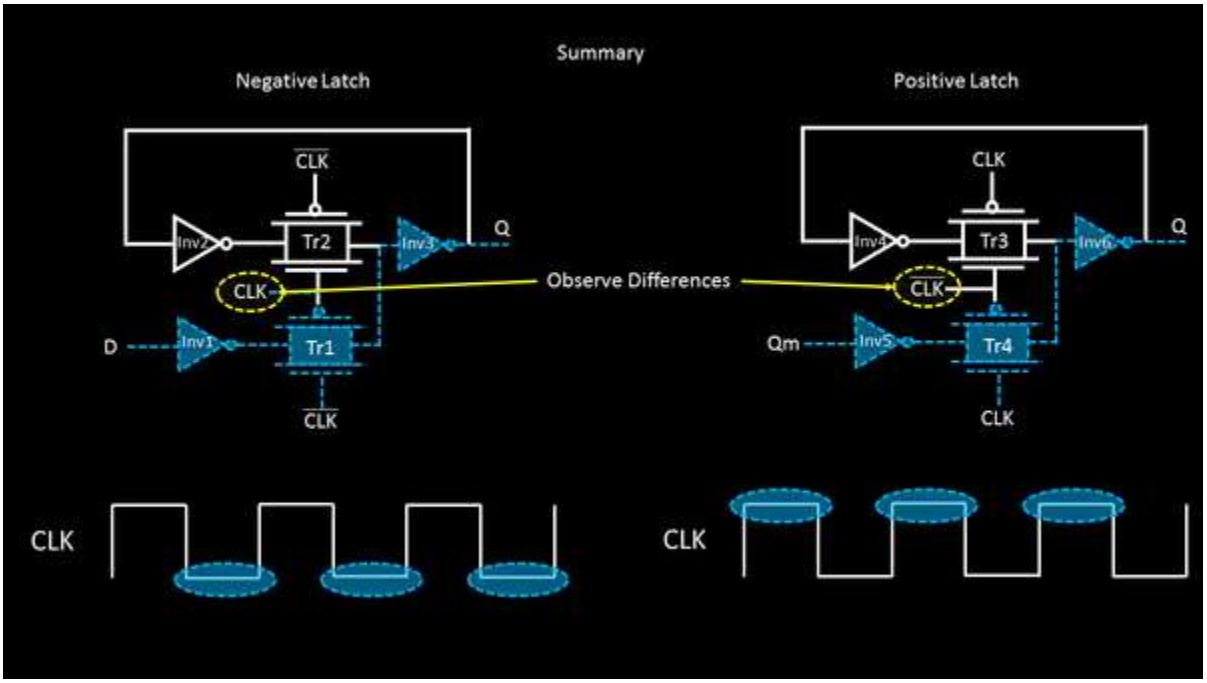

Positive Latch
CLK
Inv4
Tr3
Inv6
Q
CLK
Qm
Inv5
Tr4
CLK
CLK

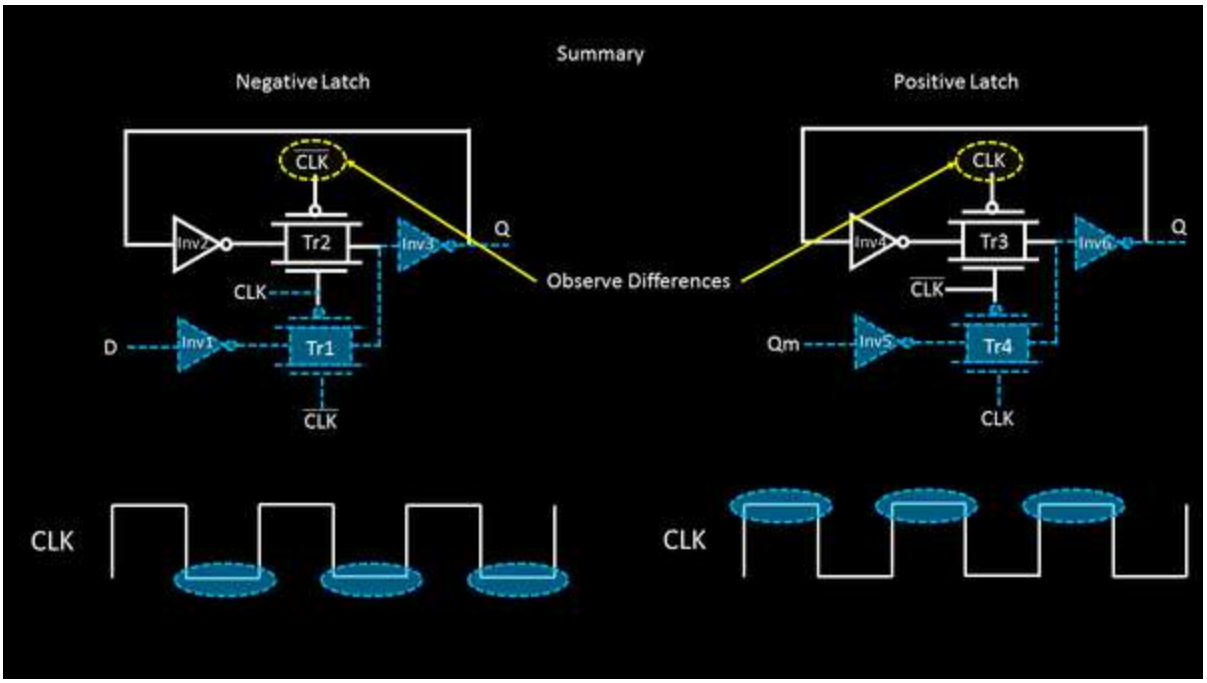

Positive Latch
When CLK is 'high', "Tr4" turns ON (i.e. PMOS/NMOS are of Tr1 are ON), and input 'Qm' is latched to output 'Q'
CLK
CLK
Inv4
Tr3
Inv6
Q
CLK
Qm
Inv5
Tr4
CLK


Summary
Negative Latch
Positive Latch
CLK
Inv2
Tr2
Inv3
Q
CLK
D
Inv1
Tr1
CLK
CLK
Inv4
Tr3
Inv6
Q
CLK
Qm
Inv5
Tr4
CLK
CLK
CLK


Summary
Negative Latch
Positive Latch
CLK
Inv2
Tr2
Inv3
Q
CLK
D
Inv1
Tr1
CLK
Observe Differences
CLK
Inv4
Tr3
Inv6
Q
CLK
Qm
Inv5
Tr4
CLK
CLK
CLK

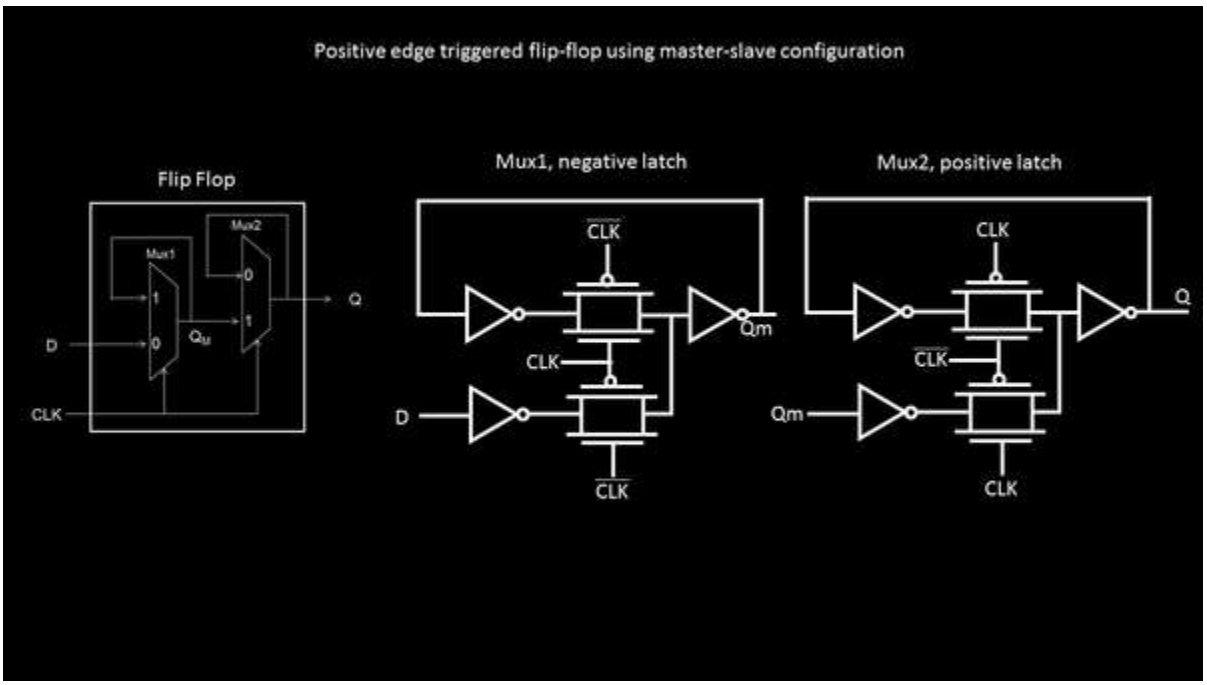

Summary
Negative Latch
Positive Latch
CLK
Inv2
Tr2
Inv3
Q
CLK
D
Inv1
Tr1
CLK
Observe Differences
CLK
Inv4
Tr3
Inv6
Q
CLK
Qm
Inv5
Tr4
CLK
CLK
CLK

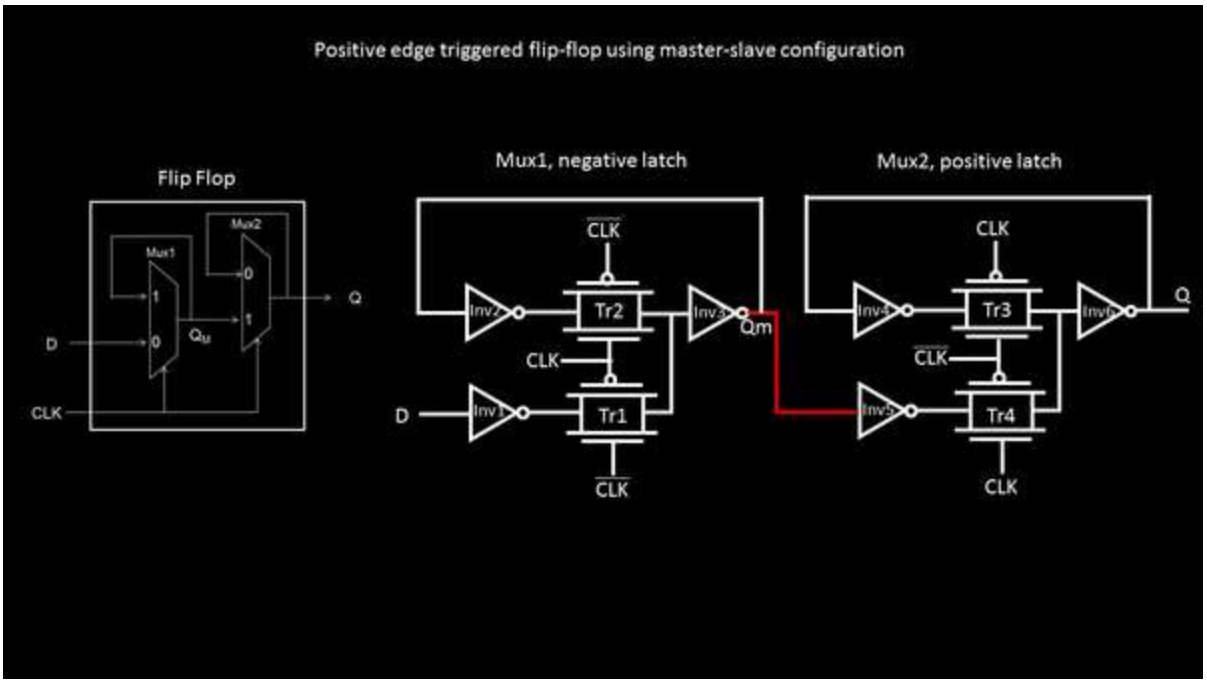

Summary
Negative Latch
Positive Latch
CLK
Inv2
Tr2
Inv3
Q
CLK
Observe Differences
D
Inv1
Tr1
CLK
CLK
Inv4
Tr3
Inv6
Q
CLK
Qm
Inv5
Tr4
CLK
CLK
CLK

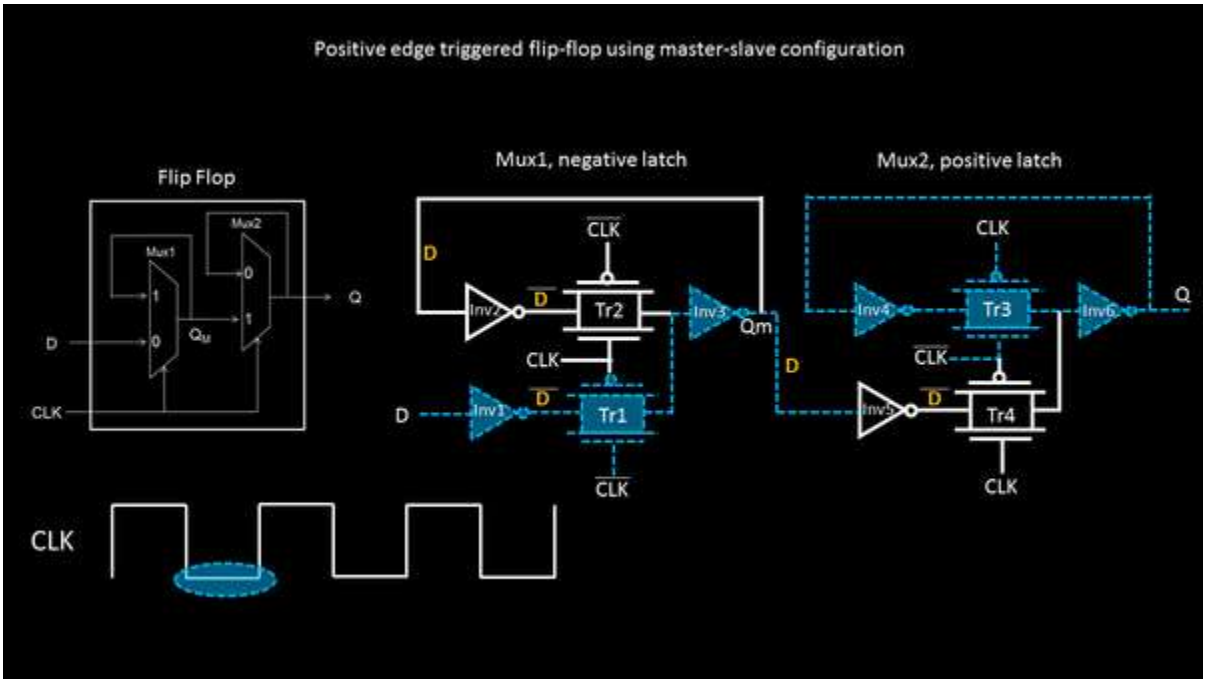



images on **transistor level implementation of flip-flop** and finally, we will nail down the 3 terms i.e. **clk-to-q delay, library setup and library hold time**.

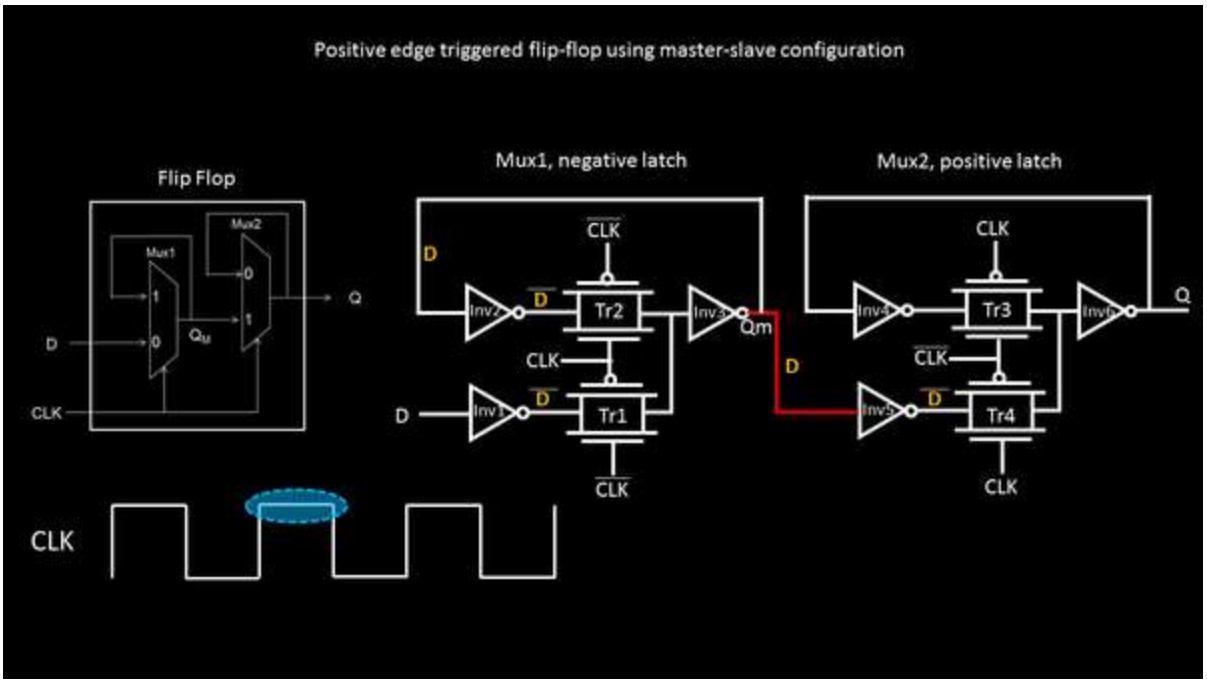
Let's begin with the **interior of flip-flop**

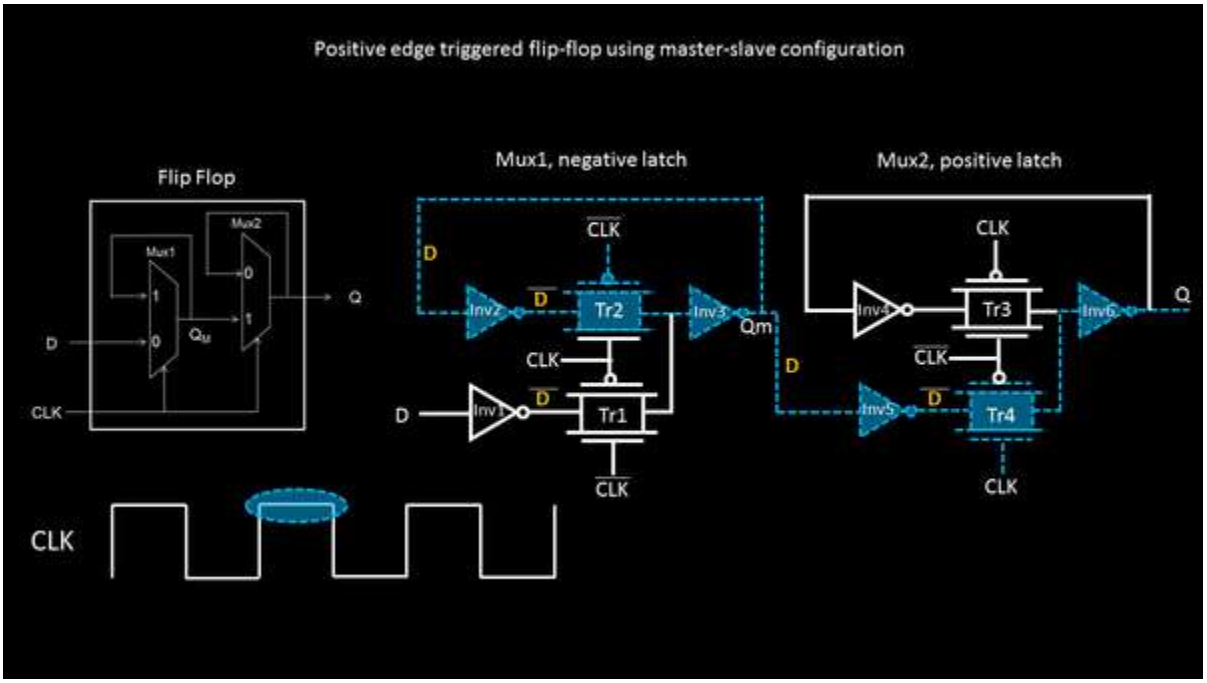





When CLK is ‘low’, “Tr1” and “Tr3” turns ON. Hence, input ‘D’ is latched to output ‘Qm’ of negative latch. ‘Inv4, Inv6’ holds the ‘Q’ state of slave positive latch Also, D_bar, is ready at output of ‘Inv5’, to propagate till ‘Q’, when CLK becomes ‘high’ **Setup Time** is the time before rising edge of CLK, that input D become valid i.e. ‘D’ input has to be stable such that Qm is sent out, to Q reliably Input ‘D’ takes at least 3 inverter delays (Inv1, Inv3 and Inv5/Inv2) + 1 transmission gate delay (Tr1) to become stable before rising edge of CLK **Setup Time** = 3 Inverter delay + 1 Transmission gate delay




When CLK is 'high', "Tr2" and "Tr4" turns ON. Hence, input 'Qm' (which is 'D' input from previous 'low' CLK) is latched to output 'Q' of negative latch, through 'Tr4' and 'Inv6' 'Inv2, Inv3' holds the 'Qm' state of master negative latch **Clk-Q delay** is the time needed to propagate 'Qm' to 'Q'.

Note, that 'D' (or 'Qm' from low 'CLK') was stable till output of 'Inv5'. So, the time required, to propagate is 1 transmission gate delay + 1 inverter delay **Clk-Q delay** = 1 transmission gate delay + 1 inverter delay **Hold Time** is the time for which 'D' input remain valid after clock edge.

In this case, ‘Tr1’ is OFF after rising ‘CLK’. So, ‘D’ can change OR can change, immediately after rise ‘CLK’ edge.

So, hold time is ‘zero’ **Hold Time = ‘zero’** And here we go, we just beat the dead horse down.