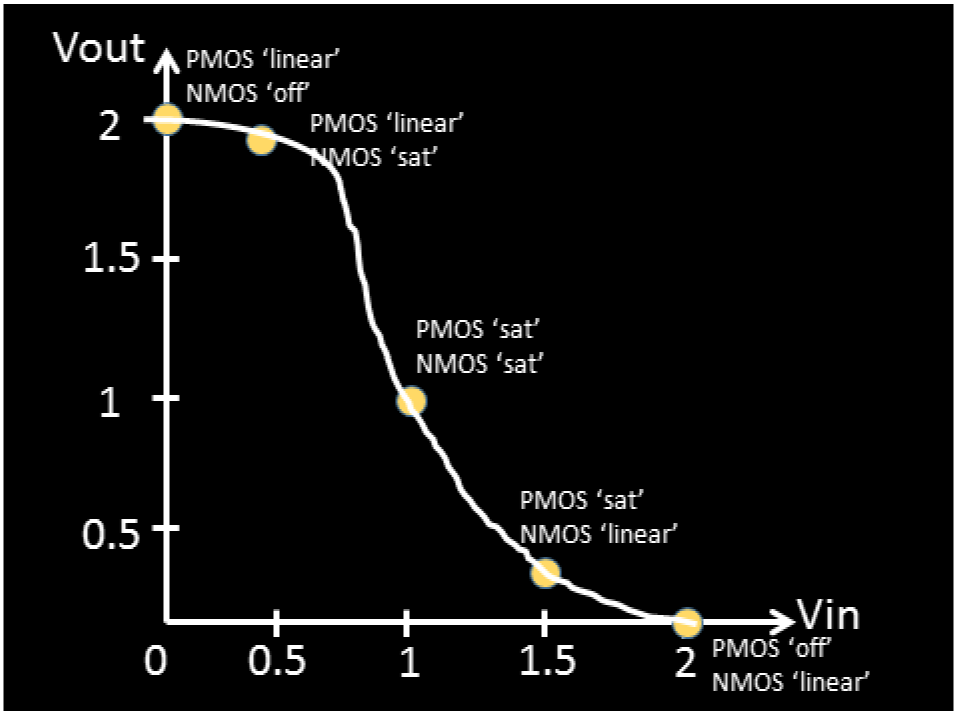
CMOS VTC- Believe it or not

YOU USE IT DAILY

Kunal Ghosh

So you are aware of the below image? No….

Well, this is **CMOS – Voltage Transfer Characteristics curve** and you use it almost daily. How? The sharpness of this curve decides how fast your cell phone is…. basically, it is used **to calculate the delay of any logic gate**. Stay with me and I will show you how….



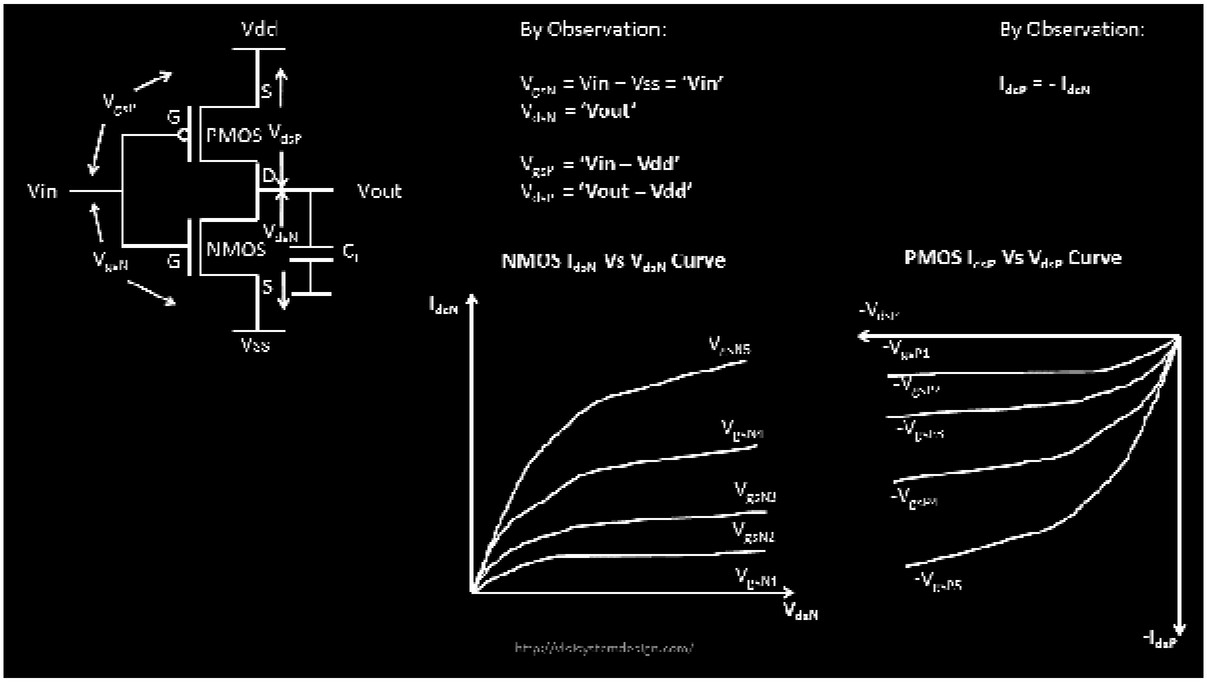
With that introduction, let me first show you (and most of you might already know), the above curve is derived (using well defined steps) from **NMOS/PMOS Id-Vd curves**.

Now, is that surprising? Well, 'yes' and 'no'. Why 'no'? Because, **CMOS is built using NMOS/PMOS**, so obviously, it will have connection with their characteristics

Why 'yes'? Because, what I have showed you, till now, through my videos or posts, is the, **NMOS/PMOS drain current (Id) and drain voltage (Vds) characteristics based on constant gate-voltage (Vgs)**, but the above curve is completely dependent on 'Vin' and 'Vout'

That's the catch!!! There should be some way **to convert 'Vds' and 'Vgs' as function of 'Vin' and 'Vout'**

Let's start with **basic NMOS/PMOS curves**, which I believe can easily be derived using **SPICE simulations**. Below image also shows **the relationship between different 'transistor' level voltages (i.e. Vds, Vgs) and 'logic gate' level voltages (i.e. Vin, Vout)**



By Observation:

V_{gsN} = Vin – Vss = 'Vin'
V_{dsN} = 'Vout'

V_{gsP} = 'Vin – Vdd'
V_{dsP} = 'Vout – Vdd'

By Observation:

$I_{dsP} = - I_{dsN}$

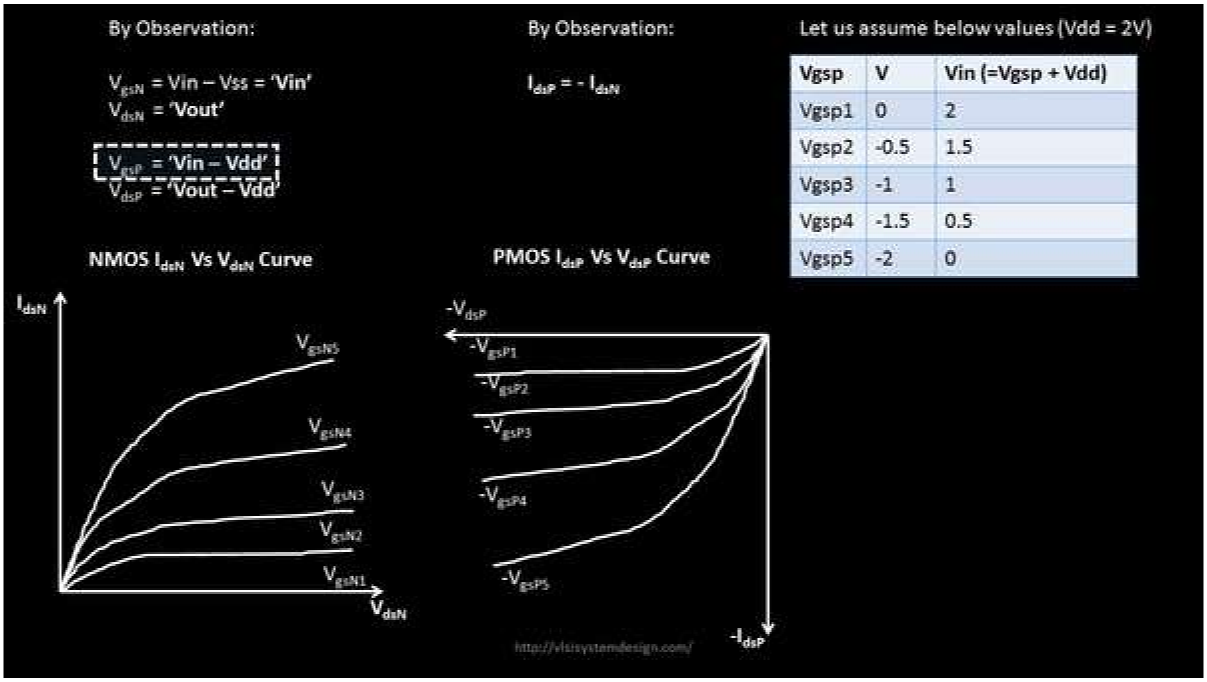
In a real world, it does makes sense to have curves which are dependent on 'Vin' and 'Vout' rather than **device level voltages** 'Vds' and 'Vgs', as most of your **PNR tools** deals with slew values which are highly dependent on 'vin' and 'vout'. They decide the voltage swing

With that background, I will show you (using the above image as reference), how do we derive the CMOS VTC in just few and easy steps.

I will derive the **CMOS VTC** in few steps, and below is the first one. We did derive the below equations sometime back, and use the same in our derivation. The goal is to get rid of all **internal node voltages like Vgsp, Vgsn**, etc, and make the curves, a function of Vin and Vout.

Why? Because the logic gates (AND, OR, INVERTER) that are given to us for usage have (in general), 4 voltages – **Vdd, Vss, Vin and Vout.** That's all we see from top, and there is no way, in **physical design and STA,** we look around the node voltages.

With that back ground, let's begin



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Let us assume below values (Vdd = 2V)

Vgsp	V	Vin (=Vgsp + Vdd)
Vgsp1	0	2
Vgsp2	-0.5	1.5
Vgsp3	-1	1
Vgsp4	-1.5	0.5
Vgsp5	-2	0

NMOS I_{dsN} Vs V_{dsN} Curve

PMOS I_{dsP} Vs V_{dsP} Curve

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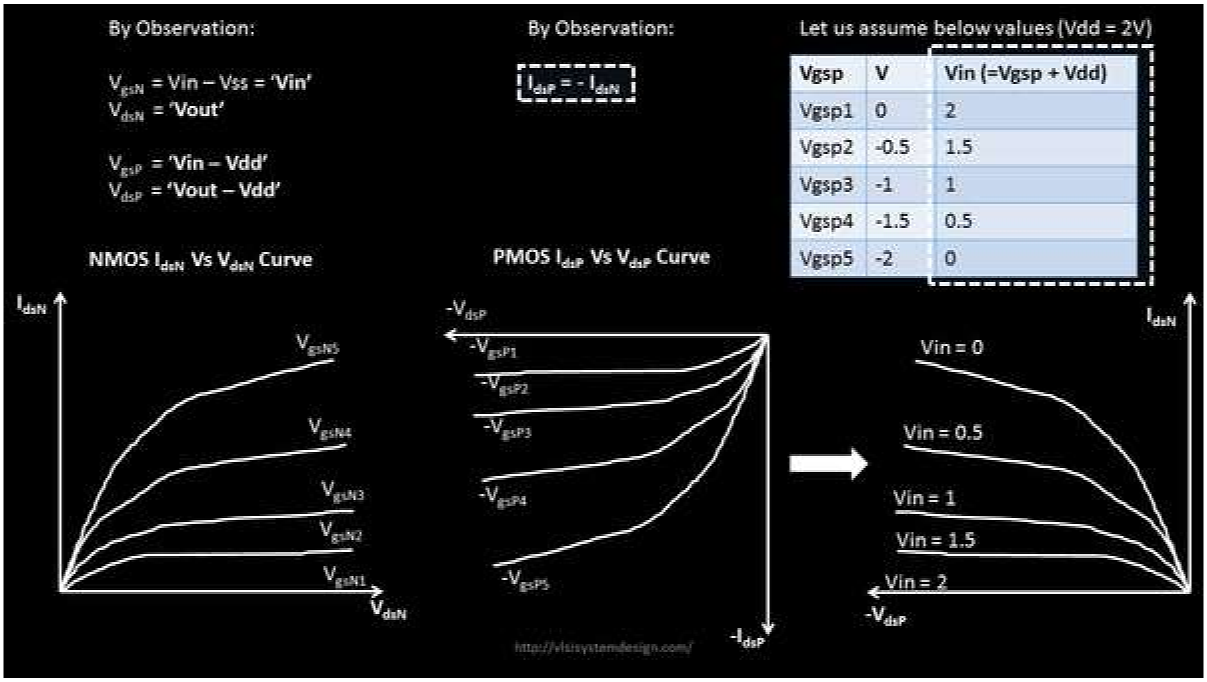
Step 1: Let's start with **PMOS and convert the node voltage 'Vgsp' to 'Vin' and shift the Idsp v/s Vdsp curve to their respective quadrant.** The table on the right top explains the conversion and now, we have an **equivalent 'Vin' for every value of 'Vgsp'**.

Also, since we have **2 kinds of currents 'Idsp' and 'Idsn'**, let's use only one of them, so every transistor will be a function of only one current and things will turn out to be simple. **Idsp = -Idsn**

With the above **conversions and logical assumptions, below (bottom right) is the curve what we get**



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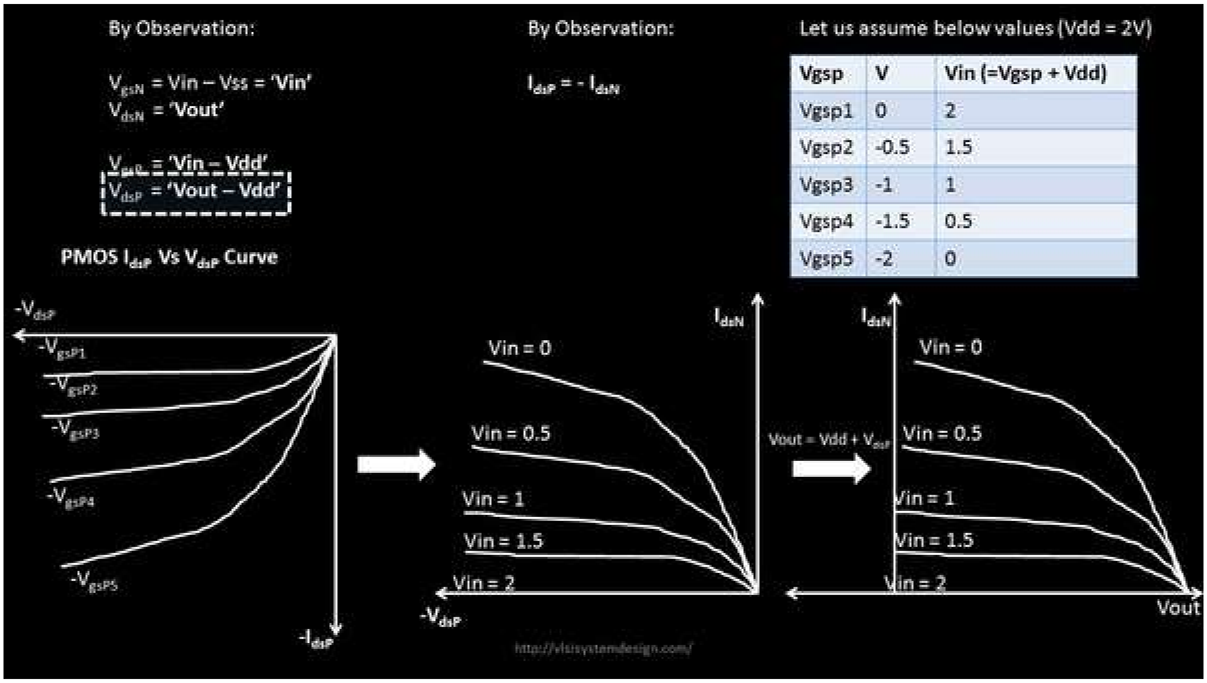
NMOS I_{dsN} Vs V_{dsN} Curve

PMOS I_{dsP} Vs V_{dsP} Curve

Also, **Vout = Vdd + Vdsp**, so let's **convert the Vdsp that's present on X axis, and then the below whole curve (bottom right), becomes completely a function of Vin and Vout**



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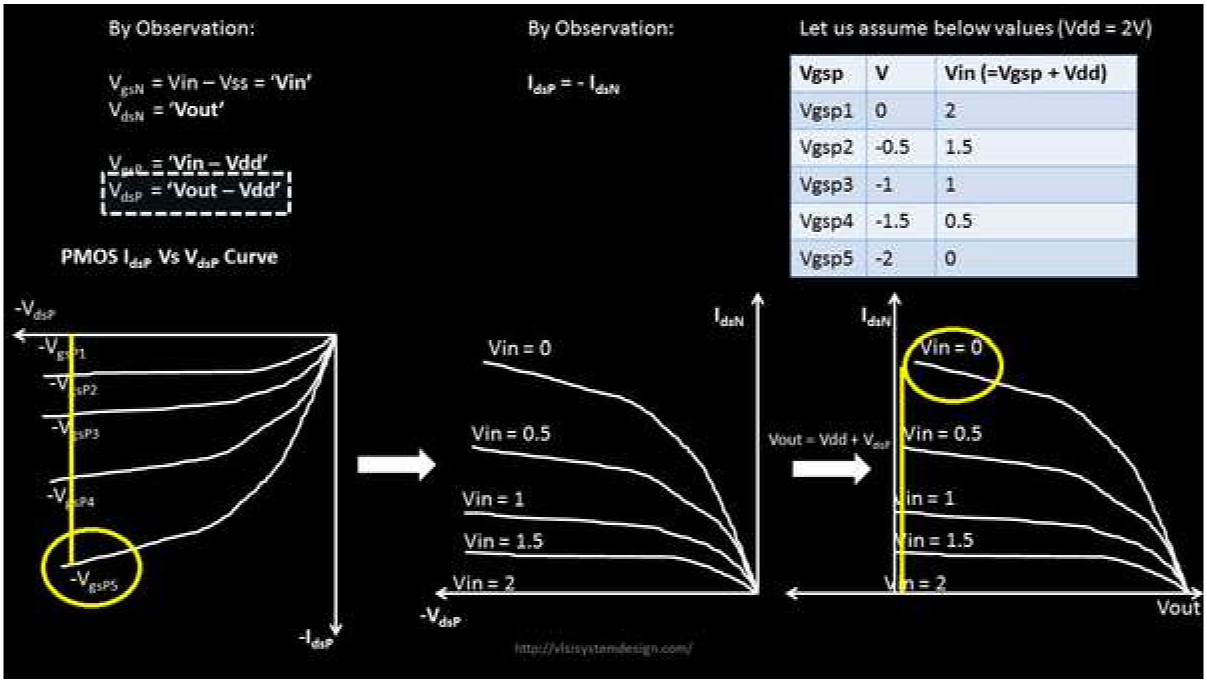
Vgsp4	-1.5	0.5
Vgsp5	-2	0

PMOS I_{dsP} Vs V_{dsP} Curve

And the above curve (bottom right), does make sense, which you can figure out by calculating the current at 1 value of Vdsp and Vgsp, and comparing the same with equivalent 'Vin' and 'Vout'

For e.g. -Vgsp5 of -2V is nothing but Vin = 0V, and -Vdsp of -2V is Vout = 0V

Now the value of **current at (Vgsp, Vdsp)** of (-2V and -2V) **is the highest saturation current -Idsp** shown below, which is nothing but +Idsn with Vin = 0V and Vout = 0V



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Vgsp5	-2	0

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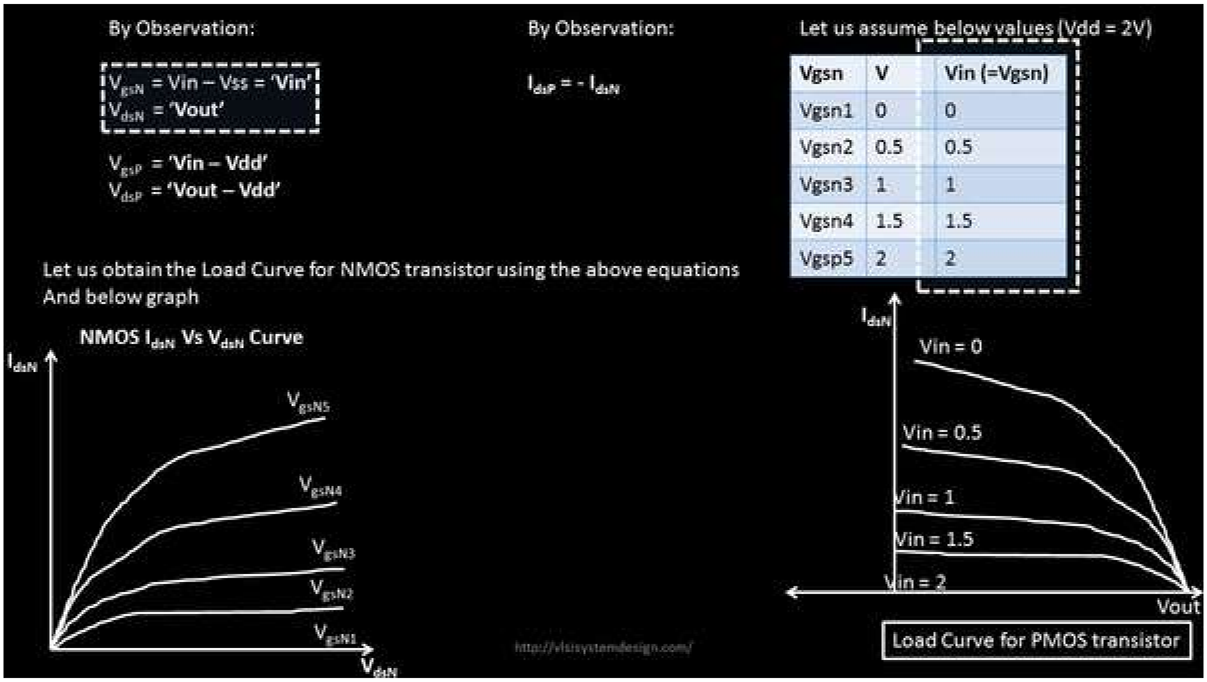
Stay with me on next post, where I will cover the Step2 and Step3 in a similar fashion, and you will realize, how easy these topics were to understand when represented in a graphical format.

we take along the **MOSFET curves,** play around with them and come up with fresh set of curves that is (eventually) being used behind all timing analysis, though its "**black box**" for users of any STA timing tool.

Now "**black box**" is what I am trying to open for you. Let's continue

The below is called the **load curve of PMOS** and its a function of only Vin and Vout (no internal voltages anymore)



By Observation:

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Let us assume below values (Vdd = 2V)

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Vgsn1	0	0
Vgsn2	0.5	0.5
Vgsn3	1	1
Vgsn4	1.5	1.5
Vgsp5	2	2

Let us obtain the Load Curve for NMOS transistor using the above equations
And below graph

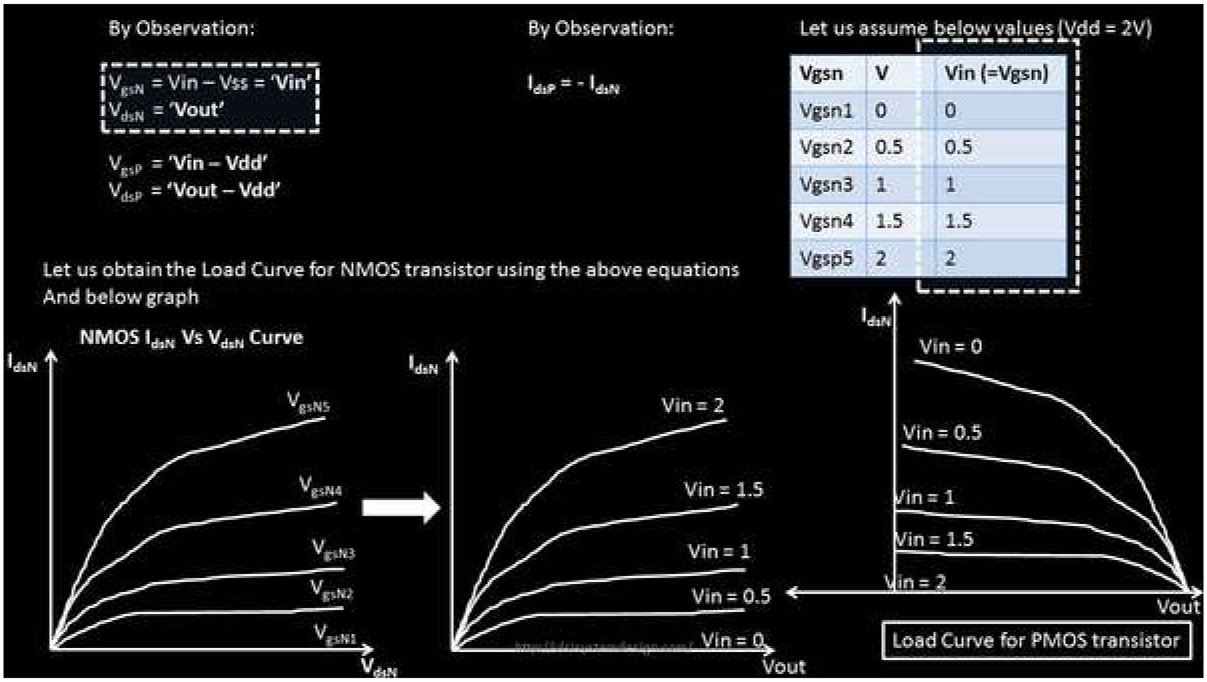
NMOS I_{dsN} Vs V_{dsN} Curve

Load Curve for PMOS transistor

Step 2: In this step, we would take the above NMOS Ids-Vds curves, and convert them as a function of 'Vin' and 'Vout'. We would use a similar approach, take the equations on top left box, and plot.

For NMOS, things are simple, as the NMOS is present at bottom of CMOS inverter, and hence, it's as good as analyzing NMOS as an independent transistor.

For e.g. 'Vgsn' becomes 'Vin' and 'Vdsn' becomes 'Vout'. It's just a matter of replacing the above voltage names and there you go!!



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Vgsn4	1.5	1.5
Vgsp5	2	2

Let us obtain the Load Curve for NMOS transistor using the above equations
And below graph

NMOS I_{dsN} Vs V_{dsN} Curve

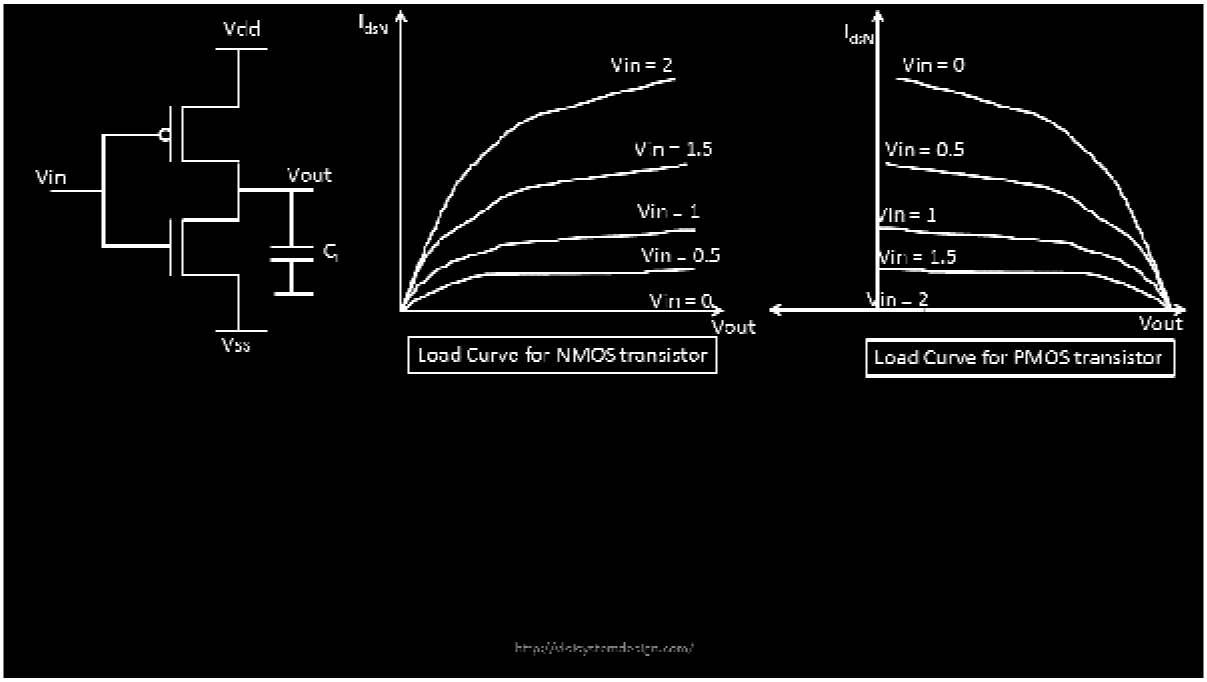
Load Curve for PMOS transistor

So, now that you have the **load curves for both transistors**, it's just a matter of just connecting the below 3 objects

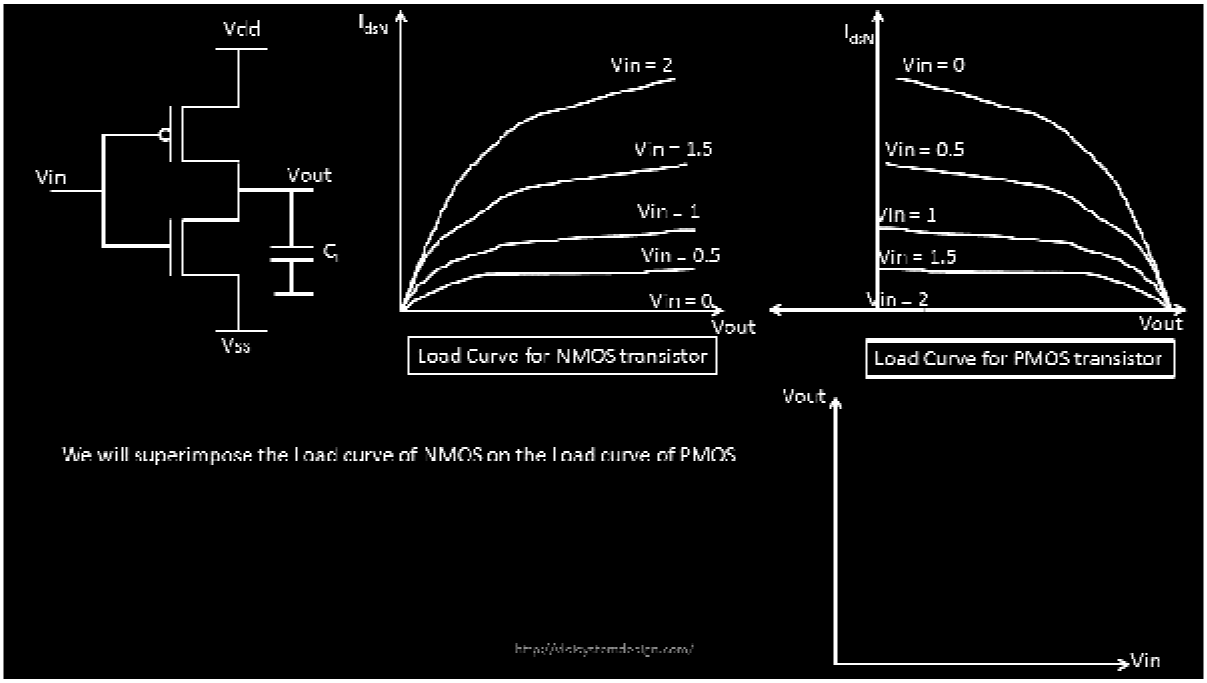
1) Load curve for PMOS transistor

2) Load curve for NMOS transistor

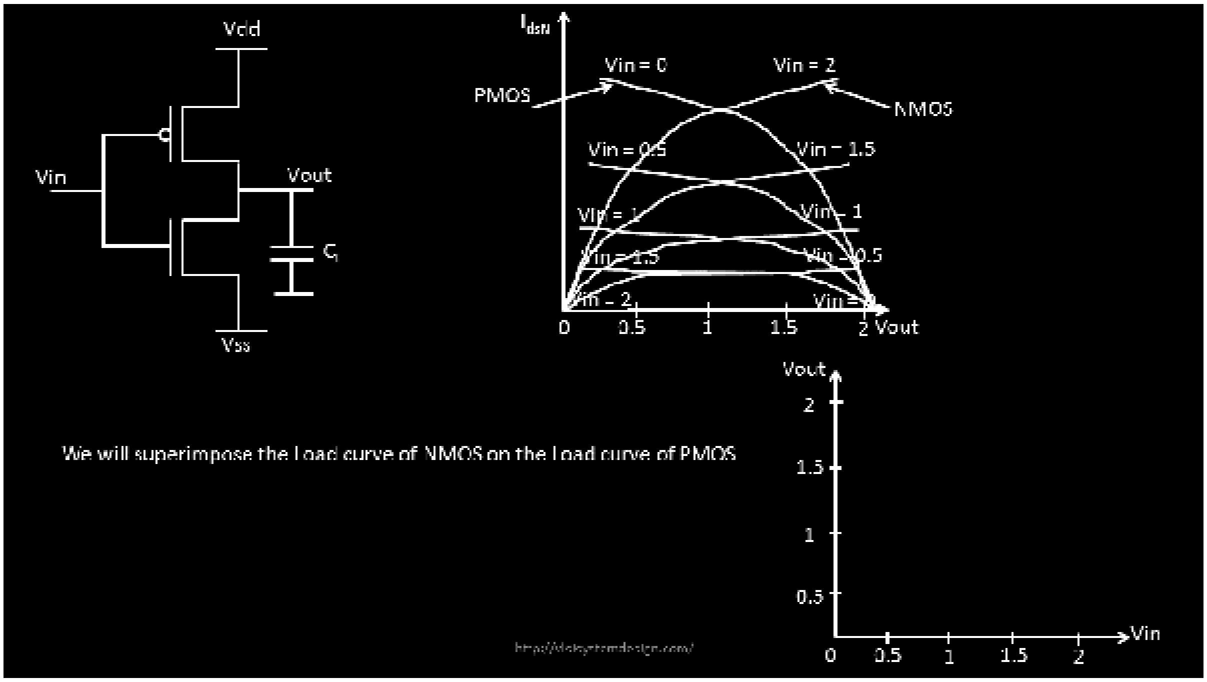
3) CMOS inverter



Step 3:
Let's **superimpose the below curves on each other** (will tell you very soon, why I am doing so), and mark the x-y axis with 0V to 2V (as that's the highest voltage we are analyzing this circuit for)



We will superimpose the Load curve of NMOS on the Load curve of PMOS



We will superimpose the Load curve of NMOS on the Load curve of PMOS

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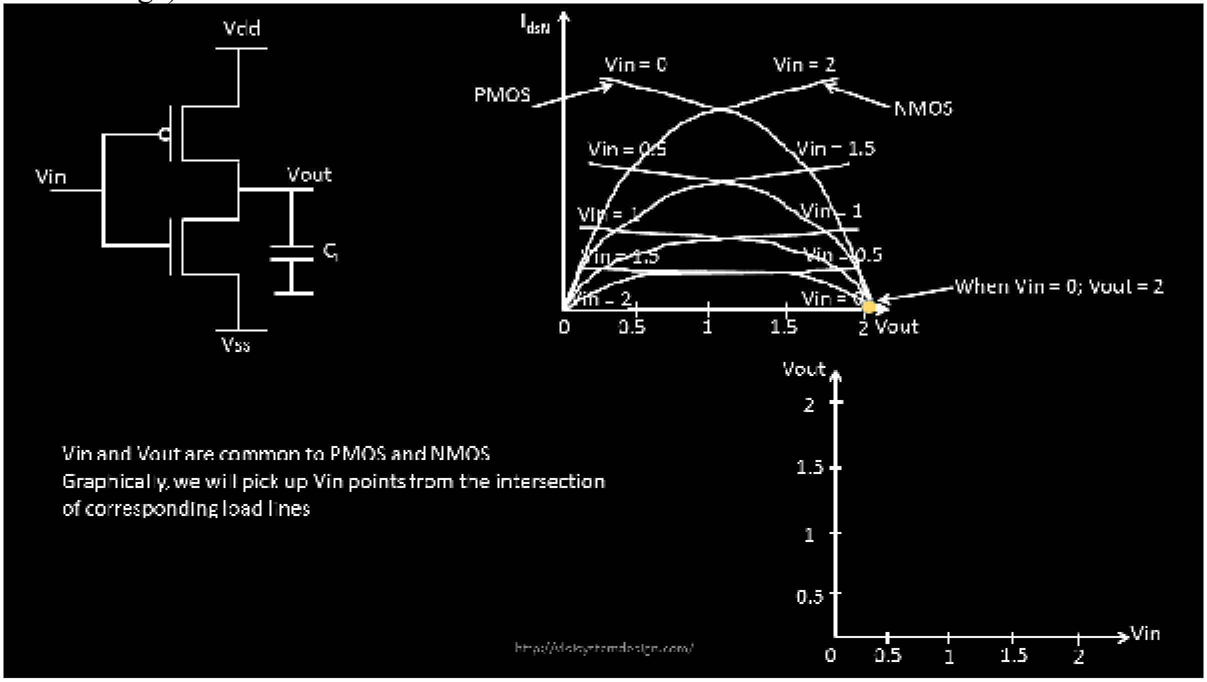
Step 4: Now, if you carefully consider the super-imposed curve and pick up the **first intersection point of Vin(PMOS) and Vin(NMOS)**, you will find that at Vin = 0V, the Vout = 2V and …. (sentence continued after below image)



Vin and Vout are common to PMOS and NMOS
Graphically, we will pick up Vin points from the intersection of corresponding load lines

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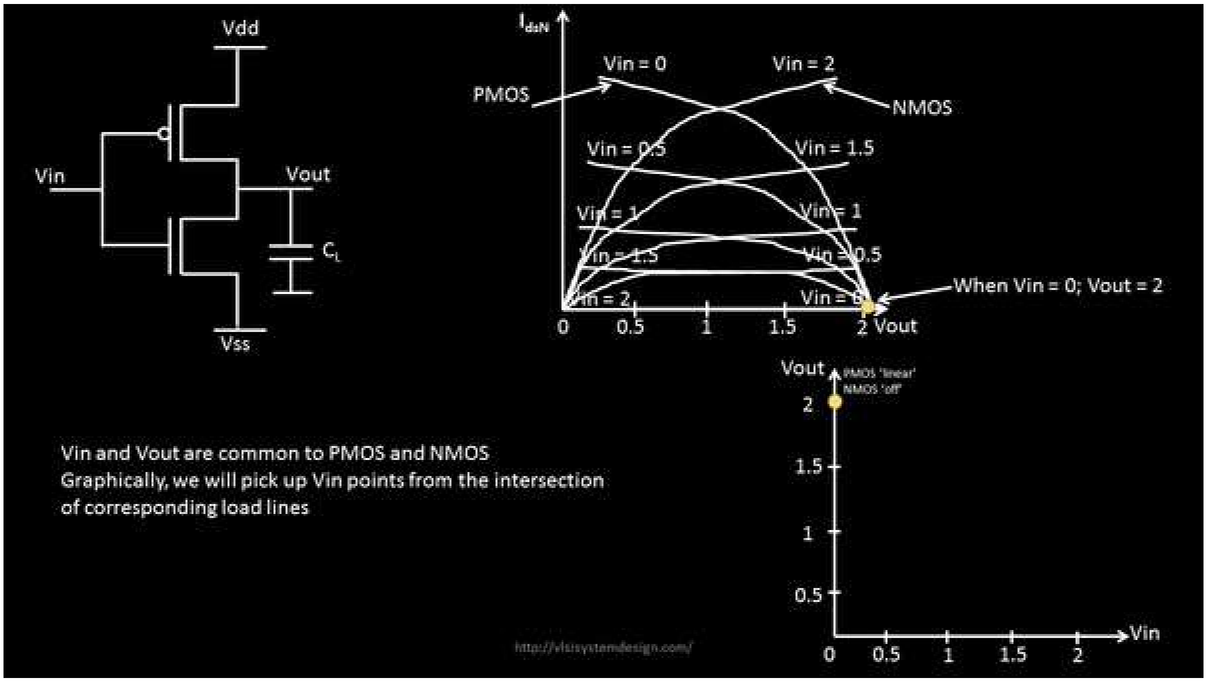
…. (sentence continued from above) and at that point, **PMOS is in linear region and NMOS is cut-off**. So, let's plot that point on the below CMOS x-y axis



When Vin = 0; Vout = 2

Vin and Vout are common to PMOS and NMOS
Graphically, we will pick up Vin points from the intersection
of corresponding load lines

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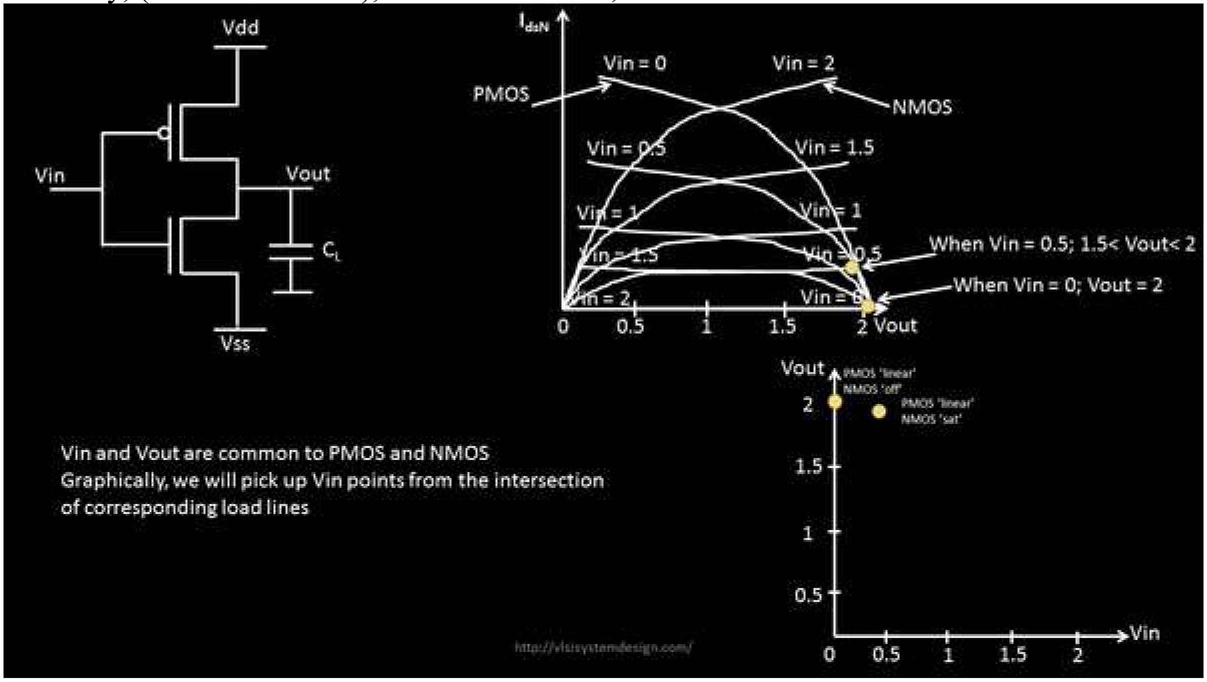
Similarly, (next intersection), when Vin = 0.5V, Vout = 1.5V to 2V



When Vin = 0.5; 1.5< Vout< 2

When Vin = 0; Vout = 2

Vin and Vout are common to PMOS and NMOS
Graphically, we will pick up Vin points from the intersection
of corresponding load lines

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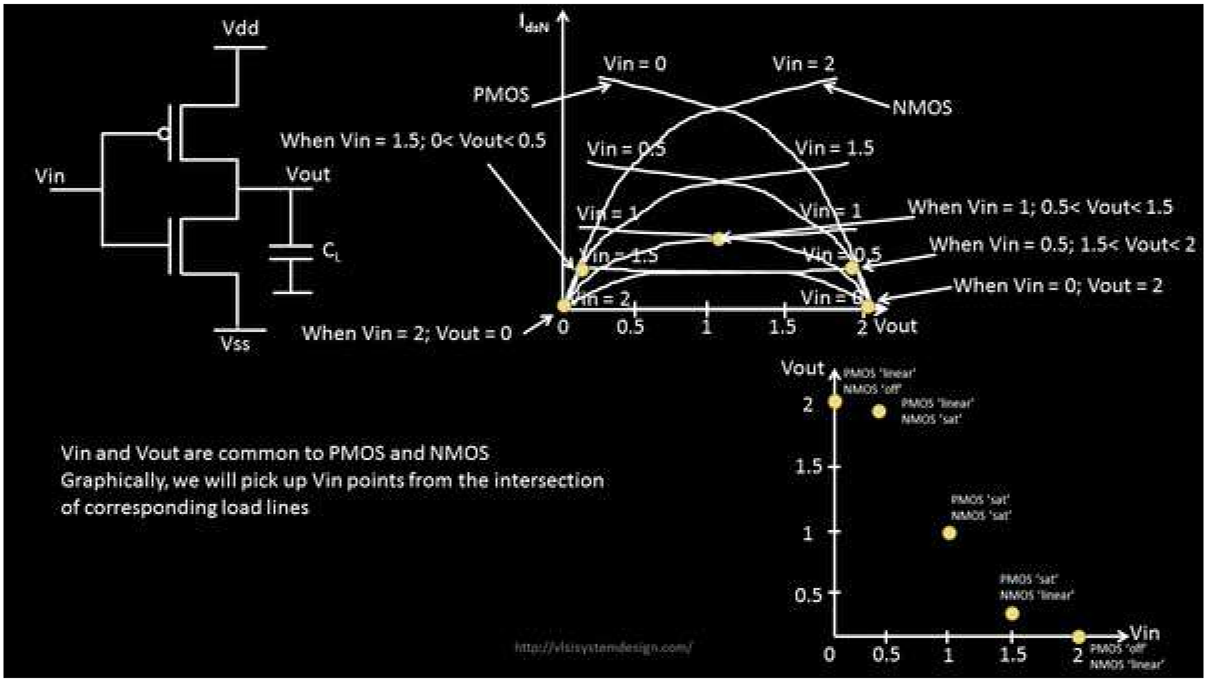
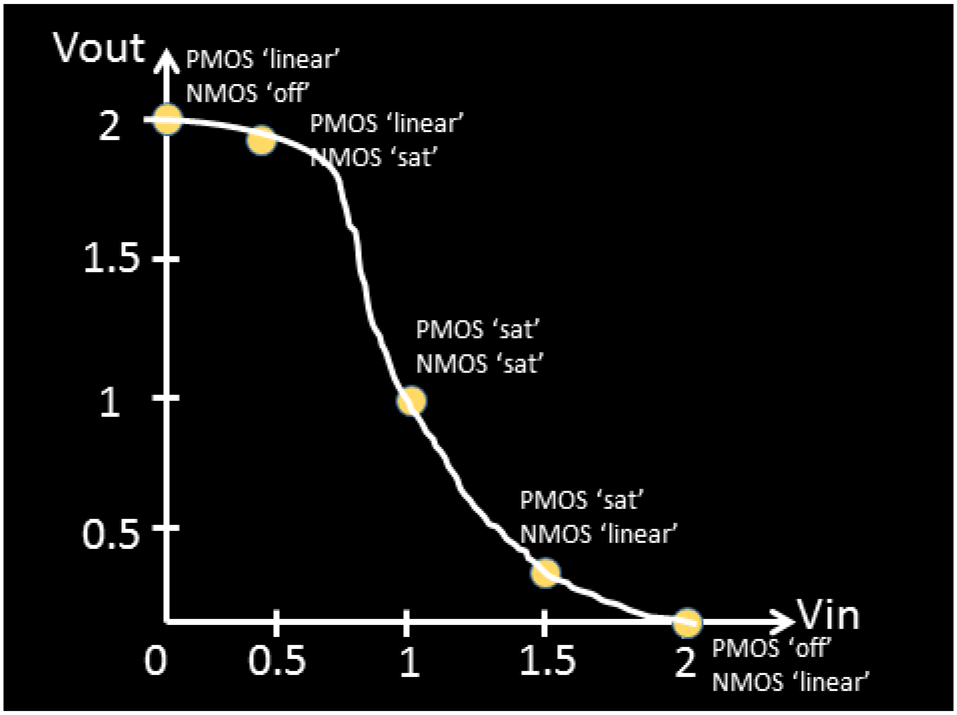
If I keep doing this for all intersection points, below is what I get



Vin and Vout are common to PMOS and NMOS
Graphically, we will pick up Vin points from the intersection
of corresponding load lines

Tadaaaa …… and there is the **CMOS VTC curve ...**..



Doesn't this curve look familiar… And don't you use this, almost, daily in all your timing analysis run? Next, is to relate this curve to delay of cell…. I will start a separate thread for that

Now that you know, from scratch, what's that is driving the delay of cells, I am sure you would look your Timing analysis from a different angle.