16-mask process

Looks complex. not anymore!!

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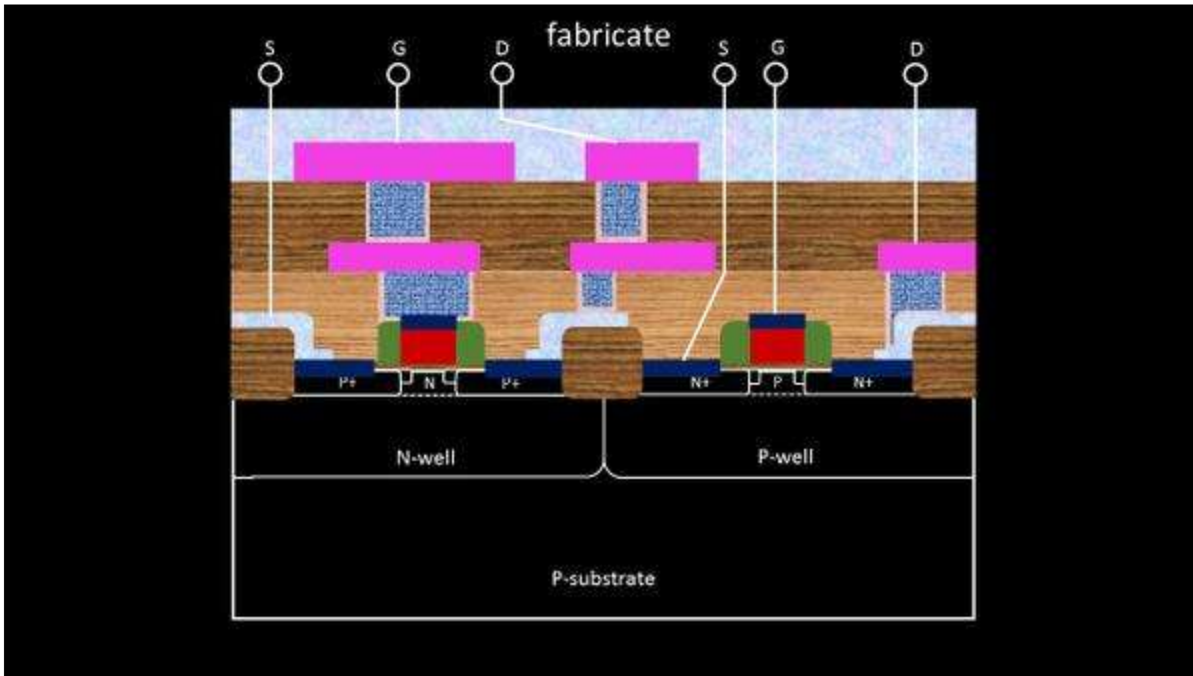


If you consider the above image, and wondering how complex it is to build and package a chip, you will change your opinion after the 16-masks that I would show in this and following blogs

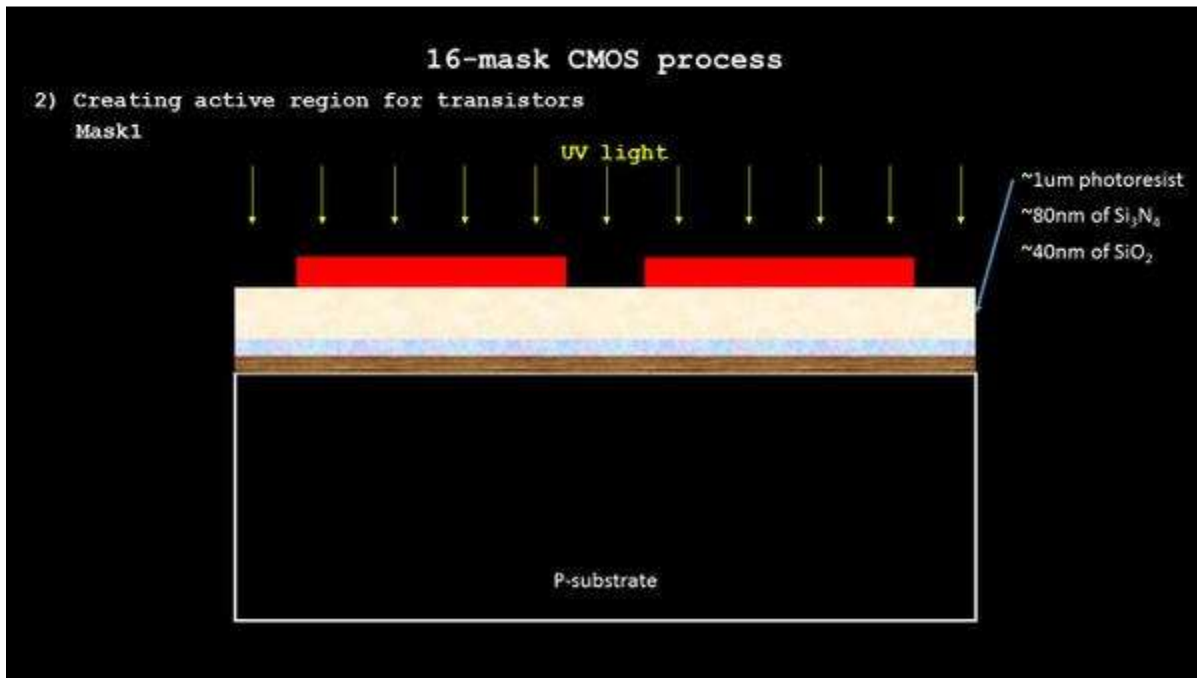
Note: The 16-mask process is also covered in detail in my new course, for which the link is below:

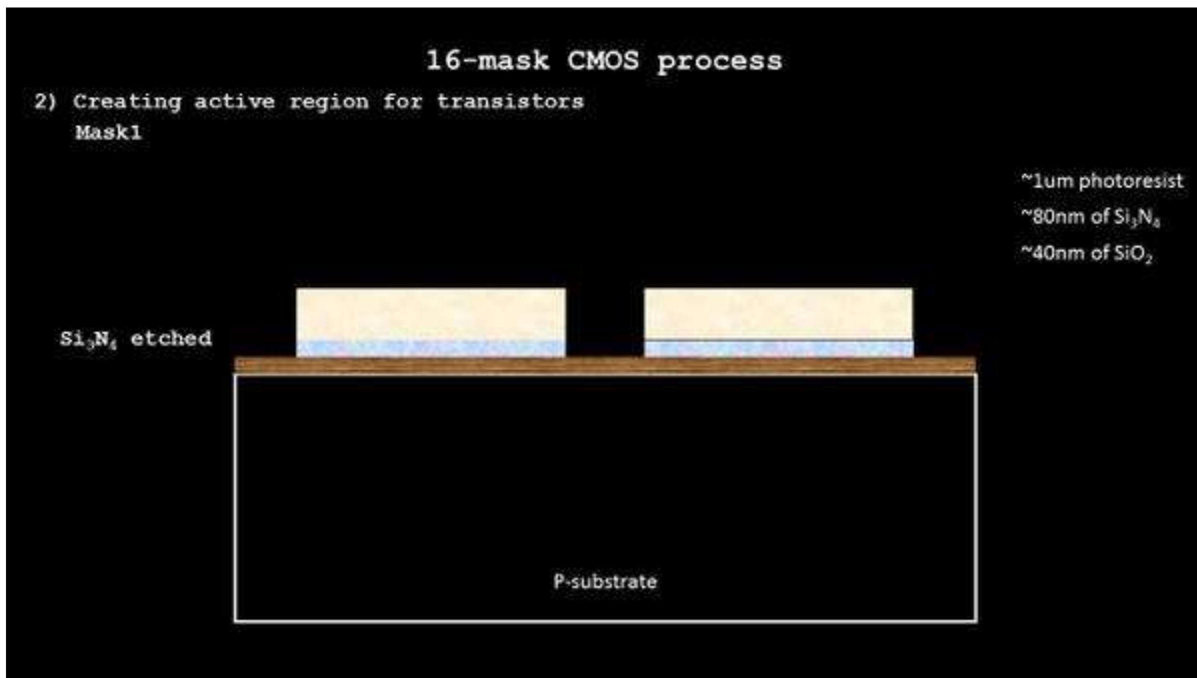
https://www.udemy.com/vlsi-academy-custom-layout

Let's skip some process steps and consider 1st mask below:

This is to create the active regions to build pmos/nmos transistors…will be evident as we move forward.

So, the mask is an opaque plate which blocks the UV light to react with certain areas of photo-resist. As shown above, part of resist is exposed to UV light, which gets washed away giving us the below open areas for further process steps, to etch away Si_3N_4:





Active regions are isolated from each other using isolation SiO2 (shown in below image), which is grown with ‘LOCOS’ technique (**Loc**al **O**xidation of **S**ilicon).

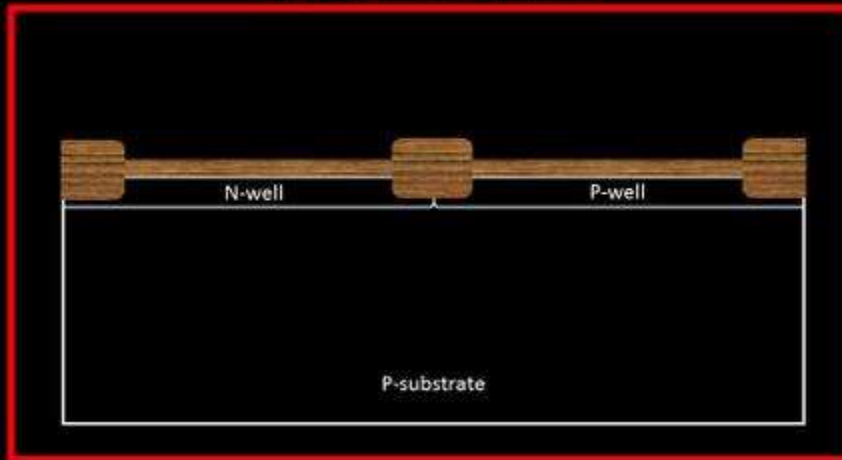
Mask2 and Mask3 will be used to create wells (nwell for pmos and pwell for nmos) as shown in below images:

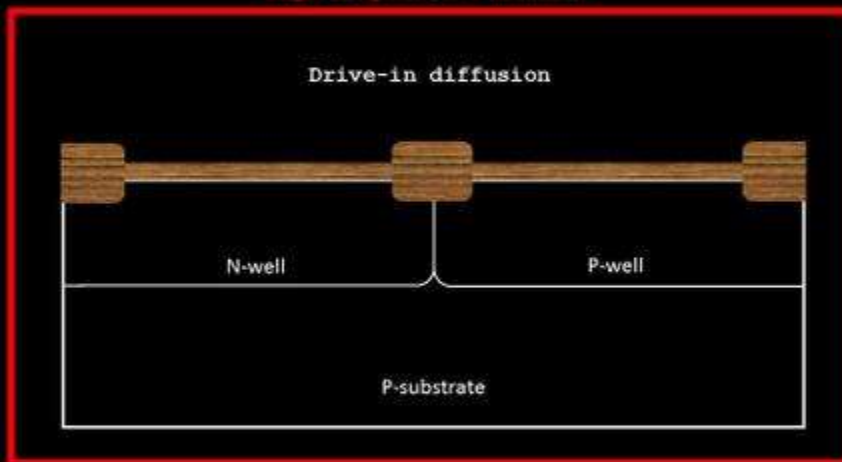
Now, if you want to relate a mask with layout, below image explains it all. Mask2 is nothing but the shaded nwell mask in a layout term

There is certain exchange of files that goes on between foundry and designers as a means of communicating design and process information. I will get back to this soon

Mask4 onwards is one where we create the most critical terminal of MOSFET i.e. gate terminal.

Once we have the nwell and pwell created, the entire structure is being placed in high temperature furnace and the ‘wells are diffused into the substrate, as shown in below 2 images





Next we fabricate the most important terminal of MOS transistor i.e. gate terminal… Remember from one of my '[Circuit design and SPICE simulation](#)' course, I had talked about some important parameters that's helpful in tuning the threshold voltage. Below image shows the same: It's the 'doping concentration' and 'oxide capacitance'

Snippet from "Circuit design and SPICE simulation" course

Threshold Voltage Equation:

$Vt = Vto + \gamma(\sqrt{|-2\Phi_f + Vsb|} - \sqrt{|-2\Phi_f|})$

Where

Vto = Threshold voltage at Vsb = 0, and is a function of manufacturing process

γ = body effect coefficient, expresses the impact of changes in body bias Vsb (Unit is $V^{0.5}$)

Φ_f = Fermi Potential

$\gamma = \frac{\sqrt{2qNA\varepsilon_{si}}}{C_{ox}}$

ε_{si} = relative permittivity of silicon = 11.7

N_A = doping concentration

q = charge of the electron

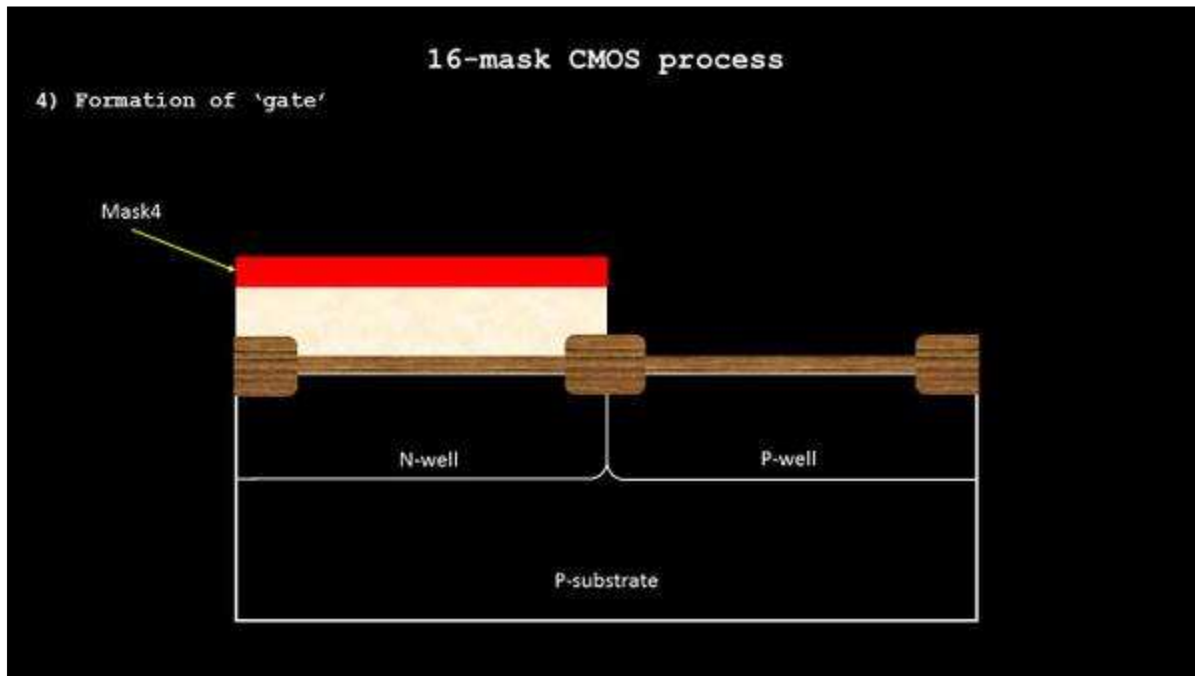
C_{ox} = oxide capacitance

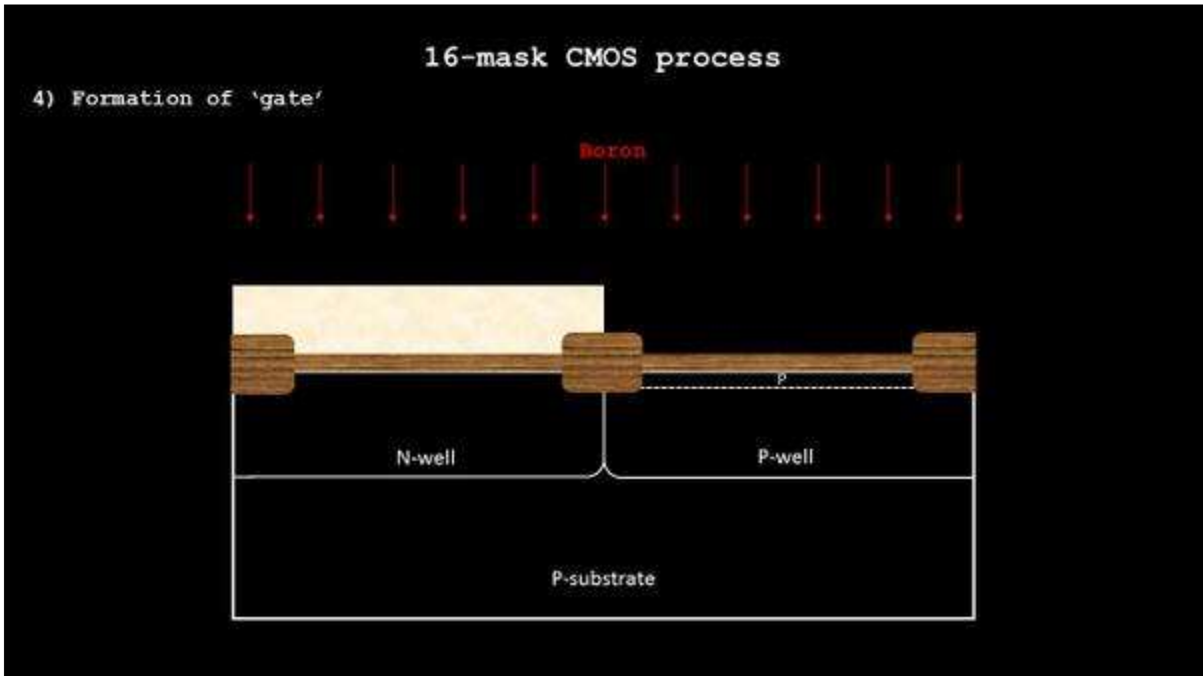
2 important terms for gate formation, as they control Vt

$\Phi_f = -\Phi_T * \ln\frac{N_A}{n_i}$

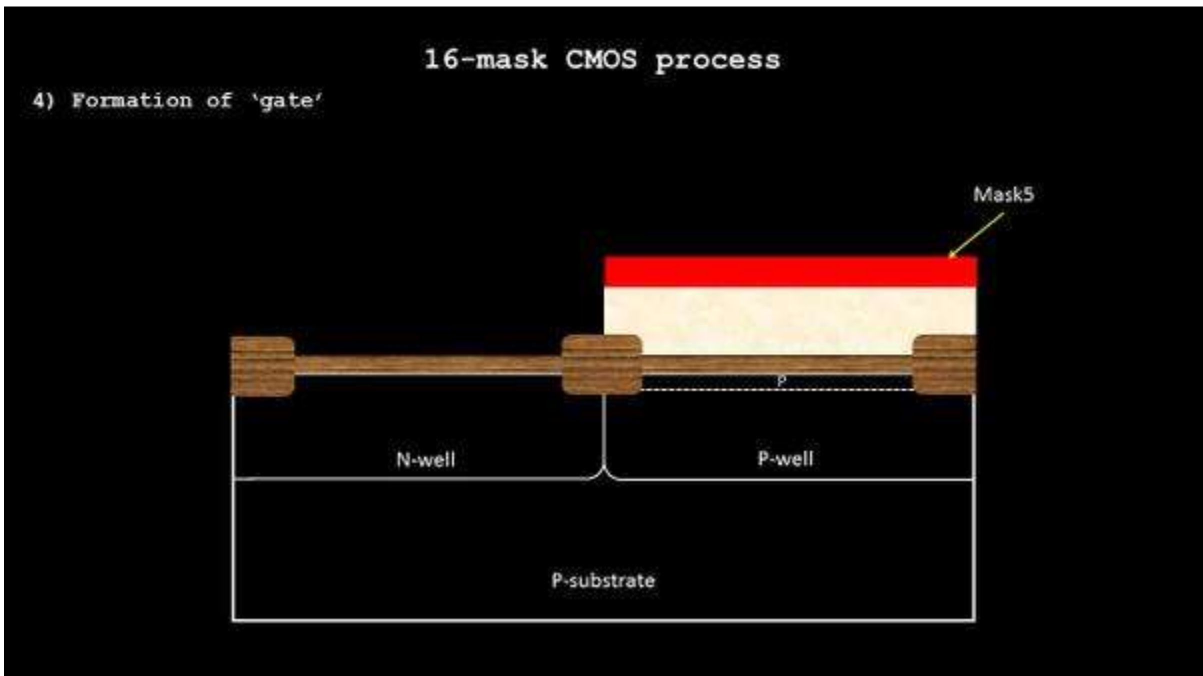
n_i = intrinsic doping parameter for the substrate

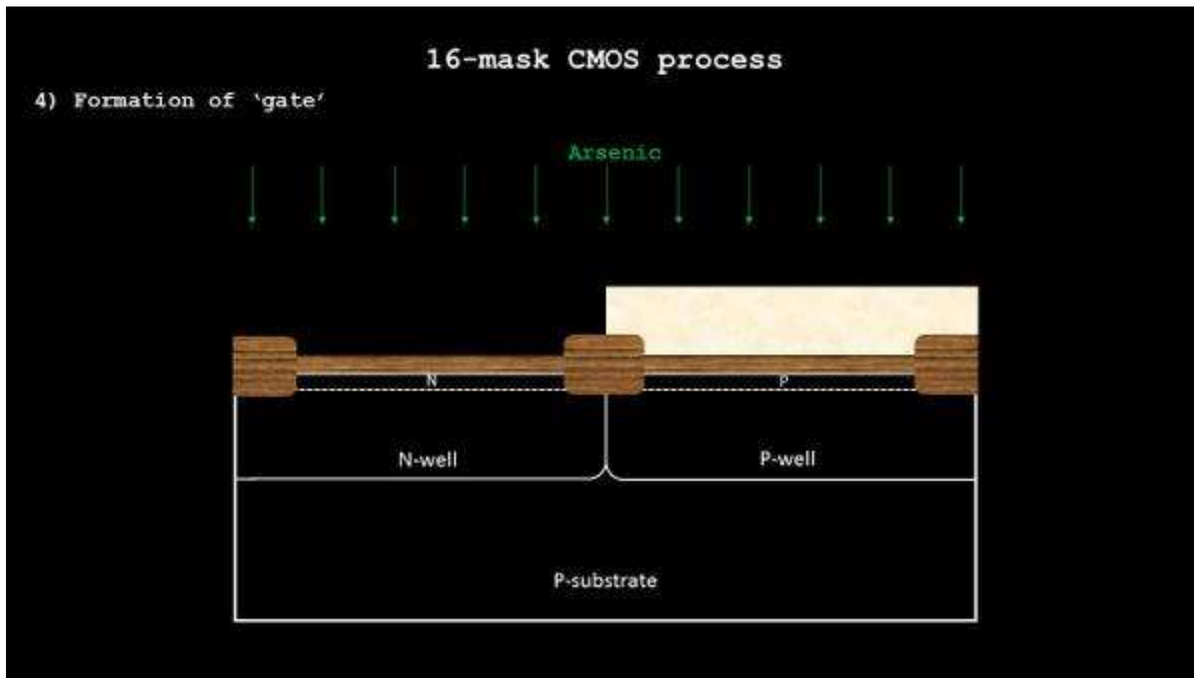
Let's see how do we attain that. And here's mask4 that helps block nwell region and dope p-well with p-type impurity i.e. boron, as shown in below images:





Similarly, we dope nwell with n-type impurity i.e. Arsenic and use mask 5 for the same as shown in below images:





The oxide present has been through lot of processes like n-type impurity doping, p-type impurity doping, nwell formation, pwell formation and so on, due to which its quality gets reduced. So, the original oxide is stripped off using HF acid and then re-grown to give high quality oxide, as shown in below image. This also helps in controlling oxide capacitance, a key parameter to control threshold voltage